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N-Channel Silicon MOSFET As A Device To Characterize MIS Structures By The BOEMDET Technique

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Abstract: *Metal-Insulator-Semiconductor (MIS) characterization is performed utilizing two n-channel Si MOSFET devices that provide both the electron tunneling current and the substrate hole current. The characterization results in parabolic electron and hole effective mass values in thermal SiO_2 of 0.42m and 0.58m respectively, the bandgap of SiO_2 of 8.9 eV and the conduction and valence band offsets of 3.2 eV and 4.6 eV. The characterization technique called BOEMDET is suited for insulators with or without bulk traps and exhibiting only Fowler-Nordheim (FN) type conduction at high electric fields. Also, the 1/E model of the anode hole injection over the hole barrier of 4.6 eV completely explains the oxide breakdown in thin oxides of 5 to 10nm at high electric fields, and having a slope constant of about 505-509 MV/cm.*

Keywords: *effective mass, FN-tunneling, band offsets, metal-insulator-semiconductor*

I. Introduction

In this report, gate tunneling electron current and substrate hole current versus gate voltage characteristics of two n^+ polysilicon gated n-channel MOSFETs are analyzed to characterize the metal-oxide-semiconductor device structure. The MOSFET data were reported by Eitan and Kolodny in 1983 and Rasras et al. in 2001. The first device has a thermal oxide of 8.5 nm and a substrate bias of -1V [1]. The second device has a thermal oxide of 7.7nm and the substrate is grounded [2]. The analysis on the device data provide the electron and hole effective masses in the thermal silicon dioxide, the conduction and valence band offsets to the oxide band edges, and the bandgap of the SiO_2. This MIS characterization can be generalized to any dielectric other than SiO_2 that contains negligible bulk traps, so as to exhibit only Fowler-Nordheim type current-voltage characteristics. Any significant amount of bulk traps will result in Poole-Frenkel type conduction. For a dielectric containing bulk traps, photoemission techniques are suited for determining the band offsets and bandgaps. These techniques do not interfere with the bulk traps [3, 4]. The dielectrics containing bulk traps may also exhibit FN conduction at high electric fields greater than 8 MV/cm.

Next, the author reviews his previous research efforts in this area. In the year 2000, the confirmed occurrence of Fowler-Nordheim hole tunneling in p-4H-SiC MOS device was reported [5]. The effective mass of holes in the oxide was reported as 0.35m, which was less than the electron effective mass in SiO_2 of 0.42m [6]. The anode field correction was applied later to the current-voltage data giving the hole effective mass value as 0.58m. This was reported in 2011 by the author [7]. In May-June 2014, the author characterized the MIS structure utilizing a polysilicon gated silicon n-channel MOSFET [8]. The formulation and calculations in this report required the threshold voltage for the MOSFET. An experimental value of 1.25 V was taken with the MOSFET having a substrate bias of -1V. The hole effective mass in SiO_2 obtained by this analysis was also 0.58m, as obtained earlier in p-4H-SiC MOS device [7]. In July-August 2014, the technique for MIS characterization was proposed called BOEMDET which used only the electron and hole current slope constants B_e and B_h values to characterize the MIS structure [9]. In this technique, either a pair of MOS devices or an n-channel MOSFET were proposed to be utilized for the characterization. Subsequently, it was thought that the MOSFET in inversion may have the same oxide voltage for both the electron and hole currents and this may yield erroneous hole effective mass. Therefore, only one pair of silicon MOS devices, one n-type and one p-type was proposed to be the devices of choice for the BOEMDET technique. This proposal was reported in November-December 2014, along with the applications of BOEMDET [10]. It is now clear that the voltage in an oxide without charges for electron and hole conduction in a MOSFET are different and are formulated in the present study.

Now, after renewed understanding, the MOSFET device in inversion is also thought to provide equally good MIS characterization which could be accurate if the experimental threshold voltage is used in place of the theoretical one [8, 9]. The Si n-channel MOSFET in inversion, under the new perspective is viewed as a minority accumulated MOS device, when biased well in strong inversion with the electrons also supplied from the source contact under bias. The source contact is either pulled down to the substrate bias of -1V [1] or, grounded [2]. This article characterizes the MIS structure utilizing both the MOSFETs resulting in carrier mass

values in SiO_2, band offsets and SiO_2 bandgap values. To an accuracy of one decimal place for the band offsets and bandgap of SiO_2 and two decimal places for the carrier masses in SiO_2, these values are same as reported earlier [6-9]. It thus confirms the validity of the MOSFET model for MIS characterization. It incorporates new result on the grounded MOSFET and a refined analysis of the voltage correction factor.

II. Theory:

Fowler-Nordheim (FN) electron and hole tunneling has been observed in Si and SiC MOS devices and in organic light emitting diodes [5-6, 11-12]. The FN equation models the current-voltage characteristics across a MOS device at high fields. It is given by the classical equation [13]:

$$\frac{J}{E^2} = A\exp\left(\frac{-B}{E}\right).....(1);$$

where J is the current density across the MOS device in A/cm^2, E is the oxide electric field in V/cm, and the pre-exponent A and the slope constant B are given by:

$$A = \frac{e^3 m}{16\pi^2 \hbar m_{ox} \phi_0}.....(2)$$

$$A = 1.54x10^{-6}\,\frac{m}{m_{ox}}\frac{1}{\phi_0}.....(A/V^2)$$

$$B = \frac{4}{3}\frac{(2m_{ox})^{1/2}}{e\hbar}\phi_0^{\,3/2}.....(3)$$

$$B = 6.83x10^7\left(\frac{m_{ox}}{m}\right)^{1/2}\phi_0^{\,3/2}.....(V/cm)$$

In A and B constants, e is the electronic charge, m is the free electron mass, m_{ox} is the electron or hole mass in the oxide, $2\pi\hbar$ is Planck's constant and ϕ_0 is the electron or hole barrier height expressed in electron volts. A plot of $\ln(J/E^2)$ versus 1/E, called an FN plot, gives the value of the slope constant B, from which $(m_{ox}/m)^{1/2}\phi_0^{\,3/2}$ product can be obtained. Then, with a known effective mass, ϕ_0 can be calculated, and with a known ϕ_0, the effective mass in the oxide can be calculated. The slope constant B is very sensitive to the oxide field as it is in the exponential and therefore precise determination of the oxide field is absolutely critical in the evaluation of the tunneling parameters. The $\ln(J/E^2)$ term is relatively much less sensitive to the oxide field as it is in the natural logarithm. The slope constant B can be independently used to determine the carrier effective masses, band offsets at the insulator-semiconductor surface and the insulator bandgap, without the knowledge of band offsets from photoemission spectroscopic measurements. This however is possible on the silicon substrate, where the grown or deposited dielectric film forms an abrupt interface and the intrinsic Fermi level of silicon lies very near the middle of its bandgap after the growth or deposition of the film due to negligible intrinsic defects in the silicon substrate. The slope constants for electron current B_e, and for the hole current B_h, can be obtained from the current-voltage characteristics of an n-channel MOSFET. Fig. 1 presents a n^+ polysilicon gated n-channel MOSFET device in inversion with grounded substrate.

A. Oxide voltage formulation in a polysilicon gated n-channel MOSFET

An n-channel MOSFET device in inversion requires the threshold voltage V_T as the positive charge on the gate terminal of the MOSFET to basically invert the channel with electrons and thus form a parallel plate capacitor with the gate as the anode and the channel as the cathode. This positive charge can be assumed to reside at the gate separate from the applied voltage Vg across the capacitor. Now, if Vg is a voltage applied at the gate anode, then this positive charge will enhance the field at the cathode for electron tunneling. So, in an oxide without charges, the gate voltage should be reduced by V_T, so that with charges the gate voltage is $Vg-V_T + V_T$ equal to Vg which is same as in an ideal oxide. Thus the gate voltage for electron tunneling from the cathode in an oxide without charges is $Vg-V_T$. The positive charge V_T reduces the field at the anode for hole conduction, Thus in an oxide without charges, the gate voltage should be enhanced to $Vg + V_T$, so that the gate voltage with charges is equal to $Vg+V_T – V_T$ equal to Vg, same as in an ideal oxide. Thus the gate voltage for hole injection and conduction from the anode in an oxide without charges should be $Vg +V_T$. The effect of the charges is elaborated in the author's earlier discussions [7, 10]. Based on the above explanation, the oxide voltage for gate tunneling electron current and substrate hole current for an oxide without charges is formulated next.

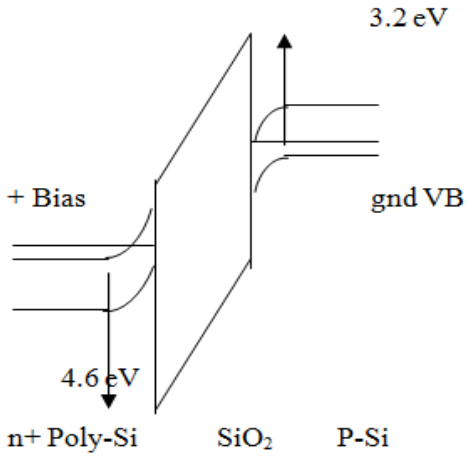

Fig.1. Energy band diagram of a n-channel Si MOSFET device in inversion.

In an ideal MOS diode, if the applied voltage across the diode is V, then $-Q_d/C_i$ is the voltage across the oxide [14]. For an n-channel MOSFET Q_d is negative, giving a positive voltage across the oxide insulator. The threshold voltage for strong inversion, V_T for a practical MOS device is expressed as:

$$V_T = \varphi_{ms} - \left(\frac{Q_i}{C_i}\right) - \left(\frac{Q_d}{C_i}\right) + V_{sinv} \quad (4)$$

where, φ_{ms} is the metal-semiconductor work function difference, Q_i is the oxide insulator charge density, C_i is the oxide insulator capacitance per unit area, Q_d is the depletion charge density in the semiconductor, and V_{sinv} is twice the bulk potential in the semiconductor at which strong inversion occurs for the MOS device. For an applied voltage V_T across the MOS device, ideally $-Q_d/C_i$ will fall across the oxide. So, the voltage across the oxide $-Q_d/C_i$ can be expressed as:

$$V_{ox} = V_T - V_{fb} - V_{sinv} \quad (5)$$

Where $V_{fb} = \varphi_{ms} - (Q_i/C_i)$ is the flatband voltage. Next, if the applied voltage is $V - V_{sb}$, then the expression for the oxide voltage becomes:

$$V_{ox} = V - V_{sb} - V_{fb} - V_{sinv} - V_{poly} + \frac{Q_{inv}}{C_i}. \quad (6)$$

Here, V_{sb} is the reverse bias applied to the substrate of a MOSFET. It is used to control the threshold voltage in a MOSFET, V_{poly} is the polysilicon depletion potential that can increase to 0.97V equal to its bandgap, when the MOSFET is biased well into strong inversion [15], and is more appropriately placed in the expression for V_{ox} instead of V_T because polysilicon depletion increases at higher applied voltages. The value of 0.97 V is derived from the fact that there is a 150meV band gap narrowing in 5 x 10^{19}/cm^3 doped Si [16], and assuming that Si and polysilicon have the same band gap of 1.12 eV. Q_{inv}/C_i is the potential drop in the electron inversion layer in MOSFET. When the MOSFET is biased well into strong inversion, the centroid of the inversion layer can be as much as 100nm, and the potential drop in the inversion layer can be calculated to be lower than 0.05V [17]. This is small and can be ignored, although it brings a small uncertainty in the oxide voltage formula. For an n+ polysillicon gated n-channel MOSFET biased well into inversion, the applied voltage V between the gate anode and substrate cathode is positive, giving positive voltage drops V_{ox}, V_{sinv} and V_{poly}. V_{sb} and V_{fb} are negative in the V_{ox} expression and Q_{inv} is negative due to electrons as the inversion charge. Also, V_T is positive and Q_d is negative with Q_d being modified due to the application of V_{sb}. From the initial explanation for the gate voltage across the MOSFET for electron and hole conduction, the oxide voltage for gate electron tunneling is given as above and the oxide voltage for hole injection and conduction from the anode can be written as:

$$V_{ox} = V - V_{sb} + V_{fb} + V_{sinv} + V_{poly} - \frac{Q_{inv}}{C_i}. \quad (7)$$

From equation (4), (V_{fb} + V_{sinv}) is replaced by (V_T + Q_d/C_i). This is considered so that the experimental threshold voltage value determined from the linear extrapolation technique of the I_D-V_{GS} curve at small V_{DS} of 20 to 50 mV in the linear region of the MOSFET channel, can be utilized to find the oxide voltage for higher accuracy. In a review article on threshold voltage determination techniques, eleven different techniques including the above are discussed with six out of eleven techniques yielding the same threshold voltage in the

studied long-channel MOSFET [18]. It has been shown in the author's previous work, that the experimentally determined V_T by the above technique gives precise results of carrier masses [8, 9]. The above modification and ignoring Q_{inv}/C_i will change the equations (6) and (7) for the oxide voltage as below:

$$V_{ox} = V - V_{sb} - V_T - \frac{Q_d}{C_i} - V_{poly} . \quad (8)$$

$$V_{ox} = V - V_{sb} + V_T + \frac{Q_d}{C_i} + V_{poly} . \quad (9)$$

By considering V_{poly} to be part of the threshold voltage equation (4), particularly for thin oxides of 5 to 10nm as in the author's previous study [8, 9], the equations (8) and (9) reduce to the author's previous formulation [8, 9], keeping in view that the V_T for a n^+ polysilicon gated n-channel MOSFET is positive and Q_d is negative. Now, for a particular technology V_{sb} may or may not be employed. V_{fb} depends mainly on the metal-semiconductor work function difference in the silicon technology as Q_i charge density is low. V_{sinv} depends on the doping concentration of the p-well which is $10^{18}/cm^3$ for the twin tub Si CMOS technology [19]. The V_{poly} will exist only in case of polysilicon gates and will be absent for a metal gated MOSFET device. The electron tunneling across the oxide is represented by the gate current in the n-channel MOSFET. The substrate hole current in the n-channel MOSFET is believed to be due to the back injection of hot holes from the polysilicon anode having the hole barrier of 4.6eV from the valence band of the polysilicon anode to the oxide valence band [20]. Once the hot holes come into the valence band over the barrier, the hole current follows the exp (-B/E) dependence of the FN tunneling equation (1) through the oxide.

B. Modification of the FN slope constant equations for devices on silicon

It has been observed from a recent report of Ultraviolet photoemission and Inverse photoemission spectroscopic experiments on 2nm dry thermal SiO_2 [4], that the conduction and valence band offsets from the intrinsic silicon Fermi level are 3.8 eV and 5.1 eV respectively, and the bandgap of SiO_2 is 8.9 eV [4, 21]. Taking the ratios of these values as 3.8/8.9 and 5.1/8.9 gives the electron and hole effective masses in the SiO_2 of 0.427m and 0.573m respectively. Within the experimental error of ±0.1 eV in the measurements of band offsets, the masses can be valued as 0.42m and 0.58m as reported earlier [7]. This ratio describes the ratio of the photo-emitted electron or hole kinetic energies during photoemission into the oxide conduction and valence bands as $\frac{0.5m_{ox,e}v^2}{0.5(m_{ox,e}+m_{ox,h})v^2}$ which equals $\frac{m_{ox,e}}{m}$, thus giving the ratio of electron effective mass to the sum of electron and hole effective masses. Here, v is the drift velocity of the electron or hole in the oxide. The sum of the electron and hole effective masses equals the free electron mass for the amorphous insulators and therefore the band offsets to insulator bandgap ratio equals the relative carrier effective masses.

Thus, the relative electron and hole effective masses $\frac{m_{ox,e}}{m}$ and $\frac{m_{ox,h}}{m}$ can be written as $\frac{(\phi_e + 0.55)}{E_g}$ and $\frac{(\phi_h + 0.57)}{E_g}$ when the insulator is grown or deposited on Si<100> or Si<111> surface. Here, ϕ_e is the electron band offset from silicon conduction band to oxide conduction band and ϕ_h is the hole band offset from the silicon valence band to insulator valence band and 0.55 and 0.57 eV are added respectively to coincide the band offsets from the intrinsic Fermi level of silicon. The intrinsic Fermi level E_i of silicon is given by:

$$E_i = \frac{E_c + E_v}{2} + \frac{kT}{2}\ln\left[\frac{N_v}{N_c}\right] \ldots\ldots (10)$$

where E_c is the bottom of the conduction band, E_v is the top of the valence band, N_c is the effective density of states in the conduction band, and N_v is the effective density of states in the valence band. N_c for silicon equals $2.8 \times 10^{19}/cm^3$ and N_v equals $1.04 \times 10^{19}/cm^3$ at 300K temperature [22]. Evaluating the above equation gives the position of intrinsic Fermi level of silicon about 0.01 eV above the middle of the silicon bandgap. Thus 0.55 eV is added to ϕ_e and 0.57 eV is added to ϕ_h for the conduction and valence band offsets from the intrinsic Fermi level of silicon. If B_e and B_h are the electron and hole tunneling slope constants, then the slope constant equations can be written as below:

$$B_e = 6.83x10^7\left(\frac{m_{ox,e}}{m}\right)^{1/2}\phi_e^{\,3/2}\ldots(11)$$

$$B_h = 6.83x10^7\left(\frac{m_{ox,h}}{m}\right)^{1/2}\phi_h^{\,3/2}\ldots(12)$$

Substituting for $\frac{m_{ox,e}}{m}$ and $\frac{m_{ox,h}}{m}$, the equations become

$$B_e = 6.83x10^7\left(\frac{\phi_e + 0.55}{E_g}\right)^{1/2}\phi_e^{\,3/2}\ldots(13)$$

$$B_h = 6.83x10^7\left(\frac{\phi_h + 0.57}{E_g}\right)^{1/2}\phi_h^{\,3/2}\ldots(14)$$

$$E_g = \phi_e + \phi_h + 1.12\ldots\ldots(15)$$

The equations (13), (14), and (15) form three non-linear simultaneous equations with three unknowns that can be solved with a simple MATLAB software program or by trial and error for a given B_e and B_h values. This evaluation will result in the values of ϕ_e , ϕ_h and E_g. Following this evaluation, the band offsets from the intrinsic silicon Fermi level can be obtained. Further, the carrier effective masses and the unknown bandgap of the insulator can be determined. This technique of characterizing an MIS structure is called BOEMDET by the author [9, 10]. The character of an MIS structure can thus be described by the below mentioned Table as:

ϕ_e	ϕ_h	E_g	m_e	m_h

C. Calculation of the corrected Slope constants B_e and B_h

The corrected oxide voltages can be calculated as given in the above analysis. The slope constant B given in equation (3) is determined from the I-V characteristics using equation (1). First $\Delta ln\,(J/E^2)/\Delta\,(1/E)$ is calculated by taking at least two points on the I-V characteristics in the FN regime at high fields utilizing the applied gate voltage. This yields the uncorrected B. Next, the corrected B is calculated by dividing $\Delta ln(J/E^2)$ by$\Delta(1/E)$, with E obtained from the corrected oxide voltages corresponding to the same current density J as for the uncorrected B.

III. Results And Discussion

Two results are presented in this section. The first one highlights the difference between the experimental V_T obtained by finding the gate voltage axis intercept of the linear extrapolation of the I_D-V_{GS} curve at the point of maximum transconductance of a MOSFET in the linear region [18], and the theoretical V_T obtained from equation (4) which is the same as the I_D=0 point of the actual I_D-V_{GS} curve in the linear region. Obviously, the experimental V_T is larger than the theoretical V_T. The second result is characterization of a MIS structure giving the band offsets, carrier masses and band gap of the insulator which is thermal SiO_2 in the present study.

The experimental and theoretical threshold voltage is arrived at in rows (9) and (10) in Table I, after determining the various parameters for a 50nm thick oxide from Fig.43 of reference [23]. It can be observed that the experimental V_T is obviously larger than the theoretical one based on their definitions. If the thickness of the 50nm oxide is reduced to 8.5nm [1], then the voltage drop in the oxide given by $-Q_d/C_i$ reduces to 0.19V from 1.09 V given in row (4). The experimental V_T for the 50nm oxide with -1V substrate bias has been determined as 1.25 V as given in Fig. 43 of reference [23]. Since Q_d/C_i is -1.09 V for the same oxide, therefore $V_T + Q_d/C_i$ becomes 0.16 as given in row (12) of Table I. This is a typical value for all the technologies with different substrate/channel doping and oxide thicknesses. Adding V_{poly} of maximum 0.97 V to this value gives the voltage correction factor to the oxide voltage equations (8) and (9) as 1.13 V. This is given in row (13) of

Table I. This method for voltage correction has also been presented in an earlier study for electron conduction in the oxide [15].

Table I. Various MOSFET parameters and their values obtained for 50nm and 8.5nm thick gate oxide to provide the theoretical threshold voltage of the MOSFET.

S.No.	Parameters	50nm thick SiO_2 [23]	8.5nm thick SiO_2 [1]
1.	$\psi_s = 2\psi_b = 2\frac{kT}{q} ln\left(\frac{N_A}{n_i}\right)$	0.7 V with $N_A=10^{16}/cm^3$ and $n_i=1.45 \times 10^{10}/cm^3$	0.7 V
2.	$Q_d = -\sqrt{2q\varepsilon_s N_A(\psi_s - V_{sb})}$	-7.55×10^{-8} Coul/cm^2 with $\varepsilon_s=11.9\varepsilon_0$ and V_{sb} = -1V	-7.55×10^{-8} Coul/cm^2
3.	$C_i = \frac{\varepsilon_0 \varepsilon_r}{d}$	6.9×10^{-8} F/cm^2	40.6×10^{-8} F/cm^2
4.	$\frac{Q_d}{C_i}$	-1.09 V	-0.19 V
5.	$\varphi_{ms} = -(0.55 + \psi_b)$	-0.898 V	-0.898 V
6.	$Q_i = q.2 \times 10^{10}$	3.2×10^{-9} Coul/cm^2	3.2×10^{-9} Coul/cm^2
7.	$\frac{Q_i}{C_i}$	0.045 V	0.008 V
8.	$V_{fb} = \varphi_{ms} - \frac{Q_i}{C_i}$	-0.944 V	-0.91 V
9.	Theoretical $V_T = V_{fb} - \frac{Q_d}{C_i} + 2\psi_b$	0.836 V	-0.02 V
10.	Experimental V_T	1.25 V	0.35 V (expected)
11.	Theoretical $V_T + \frac{Q_d}{C_i}$	-0.244 V	-0.21 V
12.	Experimental $V_T + \frac{Q_d}{C_i}$	+0.16 V	+0.16 V (expected)
13.	Experimental $V_T + \frac{Q_d}{C_i} + V_{poly}$	1.13 V	1.13 V

The gate tunneling electron current and the substrate hole current versus the applied voltage characteristics of a grounded n^+ polysilicon gated n-channel MOSFET [2] shown in Fig.6 of reference [2] are taken as observations (V_1, I_1), and (V_2, I_2) and presented in Table II. There could be small errors in reading the values from a published article. Even a 0.1 V reading error has significant change in the calculated slope constant values. The slope constants for the current versus oxide voltage data at high oxide fields are calculated next, as described in the theory section followed by the calculations of band offsets, bandgap of SiO_2, and the carrier effective masses in the SiO_2 by the BOEMDET technique [9, 10]. These observations and results are then tabulated below as Table II and Table III. The corrected oxide voltages V_{ox11} and V_{ox22} in Table II are calculated using equations (8) and (9) with the voltage correction factor given in row (13) of Table I as 1.13 V. The oxide voltages in

Table II are accordingly corrected by 1.13 V followed by the calculation of the corrected slope constants B_e and B_h as given in Section C of the theory. With these B_e and B_h values, equations (13), (14) and (15) are solved simultaneously to give the data of Table III to represent the MIS structure. For an accuracy of one decimal place the SiO_2 bandgap value is 8.9 eV and CB and VB band offset values are 3.2 eV and 4.6 eV. The electron and hole effective mass values are 0.42m and 0.58m to two decimal places.

Table II. Calculated slope constants from gate tunneling electron current and substrate hole current versus oxide voltage characteristics at high oxide fields in a n^+ polysilicon gated n-channel MOSFET having 7.7nm thermal oxide and grounded substrate [2].

Current Type	V_1/V_{ox11} (V)	I_1 (A)	V_2/V_{ox22} (V)	I_2 (A)	Slope constant B_e and B_h (MV/cm)
Gate tunneling electron current	8.0/6.87	10^{-8}	10.0/8.87	10^{-5}	254
Substrate hole current over anode barrier	8.4/9.53	10^{-11}	11.0/12.13	10^{-7}	505

Table III. Calculated band offsets, band gap of thermal oxide and carrier effective masses in SiO_2

Electron Band offset, ϕ_e (eV)	Hole Band Offset ϕ_h (eV)	SiO_2 Bandgap E_g (eV)	Electron effective mass m_e in SiO_2	Hole effective mass m_h in SiO_2
3.205	4.558	8.883	0.422m	0.577m

The voltage correction factor of 1.13 V has also been applied to the I-V characteristics of a n-channel MOSFET having -1V substrate bias [1, 8]. The MIS characterization for this device also resulted in similar values as given in Table III for the grounded MOSFET to the same accuracy of one decimal place for the bandgap and band offset values and two decimal places for the carrier effective mass values. This result is presented in Table IV and V below. The earlier study [1, 8] had assumed a V_{poly} of 0.9 V instead of the present 0.97 V as part of the threshold voltage of 1.25 V to give a correction factor of 1.06 V.

Table IV. Calculated slope constants from gate tunneling electron current and substrate hole current versus oxide voltage characteristics at high oxide fields in a n^+ polysilicon gated n-channel MOSFET having 8.5nm thermal oxide and a substrate bias of -1V [1].

Current Type	V_1/V_{ox11} (V)	I_1 (A)	V_2/V_{ox22} (V)	I_2 (A)	Slope constant B_e and B_h (MV/cm)
Gate tunneling electron current	8.0/7.87	10^{-8}	9.45/9.32	10^{-6}	253
Substrate hole current over anode barrier	9.47/11.60	10^{-9}	11.0/13.13	10^{-7}	509

Table V. Calculated band offsets, band gap of thermal oxide and carrier effective masses in SiO_2

Electron Band offset, ϕ_e (eV)	Hole Band Offset ϕ_h (eV)	SiO_2 Bandgap E_g (eV)	Electron effective mass m_e in SiO_2	Hole effective mass m_h in SiO_2
3.201	4.581	8.902	0.421m	0.579m

Two different types of samples are proposed by the author for the MIS characterization. One, a pair of n-MOS and p-MOS Si devices in accumulation are used [10]. The second, an n-channel Si MOSFET device in inversion that provides both the electron and hole current [8]. It is believed that for exact calculations, a pair of MOS devices in accumulation should be preferred but it requires poly-silicon carbide gates [10]. The use of the MOSFET device will become suitable with metal gated device to remove uncertainty in V_{poly}.`

The origin of the substrate current in n-MOSFETs having thin oxide from 5 to 10nm is under debate [1, 2, 20, 24]. Eitan and Kolodny were one of the first to observe substrate hole current in n-channel MOSFET having 8.5nm oxide, and attributed the hole current to the valence electron tunneling from the Si substrate having a barrier of 4.3eV from the Si valence band to the oxide conduction band [1]. DiMaria et al. proposed later that these holes originate as hot holes from the polysilicon anode. The energy for the hot holes are provided by the FN tunneling electrons from the cathode, which have a threshold average energy of about 5eV from the

bottom of the oxide conduction band. These hot holes are concluded to be back injected from the anode over the hole barrier at the Si anode for thin oxides of 5 to 10nm. In these thin oxides, the electron transport is quasi-ballistic, so that the maximum electron energy at the anode is independent of the oxide thickness giving a thickness independent threshold [20]. More recently, the substrate holes are experimentally shown to be generated by FN-induced photons in the polysilicon gate [2]. A report after the above, refuted this process of hole generation and concluded that the generation efficiency of photons with energy above the Si bandgap energy is 10^{-4} times smaller than that of the electron-hole pairs by impact ionization [24]. The above studies, leads the author to believe that the hot holes from the anode are back injected into the oxide over the barrier [20, 25]. After coming to the oxide valence band, the hole current follows the exp (-B/E) dependence of the FN tunneling equation (1). The calculated hole effective mass based on this dependence is exactly the same as that determined from the FN tunneling of holes observed in p-4H-SiC MOS devices in accumulation [7]. This value of hole effective mass is 0.58m for a free Fermi gas model of carriers at the emitting electrode. A value of 0.57m has been used earlier as a fitting parameter in a high frequency tunnel emitter transistor model [26]. The value is also consistent with the evidence of light holes near the top of the oxide valence band [27].

The oxide breakdown in thin oxide films of 5 to 10nm is intimately related to the substrate current due to hot holes, which is proportional to exp (-B/E) at high electric fields with the slope constant B of about 505-509 MV/cm presented in Table II and IV. An n-channel silicon MOSFET when biased in inversion as shown in Fig. 1 results in FN tunneling of electrons from the cathode into the oxide due to the smaller electron barrier to oxide conduction band of 3.2 eV. They then arrive at the polysilicon anode, where they impact ionize and create hot holes. The hot holes inject over the hole barrier of 4.6 eV at the anode [20] and cause the substrate hole current through the oxide. Some holes are trapped in the oxide causing increase in the field at the cathode [7]. This results in larger electron current injection from the cathode into the oxide by FN tunneling followed by increased substrate current and hole trapping in the oxide. This positive feedback results in the oxide breakdown. The time-to-breakdown is therefore proportional to exp (-B/E) with the slope constant B of about 505-509 MV/cm instead of 350 MV/cm reported earlier [28]. This 1/E model of the anode hole injection [28] completely explains the oxide breakdown in thin oxide films of 5 to 10nm at high electric fields.

The knowledge of electron and hole effective masses and conduction and valence band offset values in a metal-oxide-semiconductor (MOS) device can facilitate simulation of FN tunneling currents through a MOS device at high fields. The FN onset field and the dielectric breakdown field can also be determined. The FN onset field can be obtained for a minimum displacement current density of 10^{-8}-10^{-9} A/cm^2, and the dielectric breakdown field can be obtained for a current density of 10^{-4}A/cm^2, with the above knowledge. The thermal SiO_2 having an electron band offset of 3.2 eV and a carrier mass of 0.42m giving a slope constant of 254 MV/cm yields a breakdown field strength of about 9.5 MV/cm in the present study. Furthermore, the onset field is the upper limit to which the oxide can work as a good insulator without injection and trapping of carriers in it. The trapping of carriers causes degradation of the oxide and reduces its reliability.

IV. Conclusion

The parabolic electron and hole effective masses in the thermal oxide are determined to be 0.42m and 0.58m for a free Fermi gas model of carriers at the emitting electrode. For this, a grounded Si n-channel MOSFET and a MOSFET with -1 V substrate bias are utilized. These carrier masses are related to the band offsets in SiO_2/Si<100> MOS devices accurately though the MOSFET model. To an accuracy of one decimal place, the SiO_2/Si<100> conduction band and valence band offsets are calculated to be 3.2 eV and 4.6 eV respectively. The SiO_2 bandgap is calculated to be 8.9 eV. A MOSFET can be utilized to characterize MIS structures with other insulating materials having negligible bulk traps or having bulk traps and exhibiting FN conduction at high electric fields with the limitation that only 5 to 10nm thick insulator can be used. The formulated oxide voltages utilizing experimental threshold voltages are considered more accurate for the characterization. Also, the 1/E model of the anode hole injection over the hole barrier of 4.6 eV completely explains the oxide breakdown in thin oxides of 5 to 10nm having a slope constant of about 505-509 MV/cm.

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