Silicon Nanowire Based MOSFET Parameter Analysis

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Abstract: *As the conventional silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches its scaling limits many novel device structures are being extensively explored. Among them, the silicon nanowire transistor (SNWT) has attracted broad attention from both the semiconductor industry and academia. To understand device physics in depth and to assess the performance limits of SNWTs, simulation is becoming increasingly important. The objectives of this paper are to assess the performance of SNWTs. A nano device simulator called fettoy was utilized for this purpose. The various output parameters analyzed were Quantum capacitance vs. gate voltage, Drain current vs. gate voltage, drain current vs. drain voltage, Drain induced barrier lowering, Threshold swing, Carrier injection velocity, on current, off current, Output conductance, Transconductance and Voltage gain for variation in input parameters like Dielectric materials, Thickness of dielectric material, Diameter of silicon nanowire and Gate Control Parameter. Also the effect of temperature was also studied.*

I.   Introduction

As the MOSFET gate length enters the nanometer regime, short channel effects (SCEs), such as threshold voltage (V_T) rolloff and Drain-Induced-Barrier-Lowering (DIBL), become increasingly significant, which limits the scaling capability of *planar* bulk or Silicon-On-Insulator (SOI) MOSFETs [1]. At the same time, the relatively low carrier mobility in silicon (compared with other semiconductors) may also degrade the MOSFET device performance (e.g., ON-current and intrinsic device delay). For these reasons, various novel device structures and materials – silicon nanowire transistors, carbon nanotube FETs, new channel materials (e.g., strained silicon, pure germanium), molecular transistors, etc all are being extensively explored. Among all these promising post-CMOS structures, the silicon nanowire transistor (SNWT) has its unique advantage – the SNWT is based on silicon, a material that the semiconductor industry has been working on for over thirty years; it would be really attractive to stay on silicon and also achieve good device metrics that nanoelectronics provides. As a result, the silicon nanowire transistor has obtained broad attention from both the semiconductor industry and academia.

Semiconductor Nano Wires (NWs) have attracted significant interest because of their potential for a variety of different applications, including logic and memory circuitry, photonics devices, and chemical and biomolecular sensors. Although many different types of semiconductor NW have been investigated, silicon NWs have become prototypical nanowire because they can be readily prepared, the Si/SiO2 interface is chemically stable, and Si NWs are utilized in a number of device demonstrations that have well-known silicon-technology-based counterparts. Various techniques have been developed to synthesize semiconductor NWs, including the materials method known as Vapor-Liquid-Solid (VLS) growth and the templating method known as super lattice nanowire pattern transfer (SNAP).

II.   Silicon Nanowire MOSFET

A nanowire is a wire having its diameter of the order of a nanometer (10-9 meter). At these scales, quantum mechanical effects are important hence such wires are also known as 'quantum wires'[2]. The nanowires could be used, in the near future, to link tiny components into extremely small circuits. Typical nanowires exhibit aspect ratios (length-to-width ratio) of 1000 or more. Silicon Nanowires (SiNWs) are currently attracting much attention as promising components for future nano-electronic devices such as nanowire based field effect transistors, photonic and optoelectronic devices, nanowire based solar cells and NW based chemical or biological sensors [3]. This is due to the fact that they show electronic, optical, chemical, mechanical, and thermal properties that differ from their bulk counterparts. Bulk Si is an indirect gap material, the SiNWs are useful one-dimensional nanostructure for tailoring its physical properties from indirect to direct band gap.
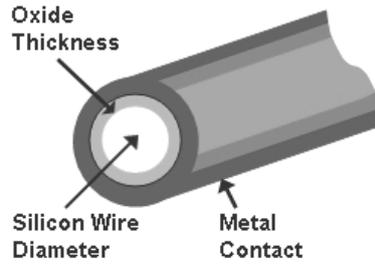
Fig.1. Structure of Silicon Nanowire transistor

Silicon nanowire transistors with various types of cross-sections are being extensively explored by a number of experimental groups. The various cross sections are the cylindrical wire (CW), triangular wire (TW) and rectangular wire (RW) nanowire FET as shown in fig 2, where T_{Si} is the silicon body thickness, W_{Si} is the silicon body width and W_{Wire} is the wire width. For the CW FET, $T_{Si} = W_{Si}$ is equal to the diameter of the circular Si body. Triangular wire nanowire FET device was built on a Si (001) wafer and the Si body layer was etched along the (111) surfaces, so the cross-section of the Si body becomes an isosceles triangle and the channel of the device is <110> oriented. At the same time, different types of tri-gate/gate-all-around FETs were fabricated by using wires with *rectangular* cross-sections. The diameters of these wire transistors are around 30-100nm and the gate lengths are >50nm. In addition, we also have the cylindrical SNWT , a gate-all around structure, which offers the optimum gate control and scaling potential among all kinds of SNWTs.

Fig. 2 The cross-sections of the various nanowire FET structures – the cylindrical wire (CW), triangular wire (TW) and rectangular wire (RW) FETs.

III.   Simulation Results and Discussion

The various output parameters were studied by varying the input parameters as shown in the Table.1

Table .1 Various input parameters and their range of variations.

Input parameters	Variation in parameters					
Dielectric material (dielectric constant)	Teflon (2.1)	Polyethylene (2.25)	SiO2 (3.9)	ZrO2 (15)	HfO2 (25)	TiO2 (40)
Dielectric thickness	1.5nm	3nm	6nm	9nm		
Diameter of SNW	1nm	5nm	10nm	15nm		
Gate control parameter (GCP)	0.1	0.3	0.5	0.8	0.88	0.92
Temperature	273K	300K	325K	350K	375K	400K

3.1. Quantum capacitance Vs Gate voltage

The Simulations were carried out to obtain the quantum capacitance for a sweep in gate voltage (0 to 1V) in a silicon nanowire MOSFET with Drain voltage as 1V and variations in input parameters.

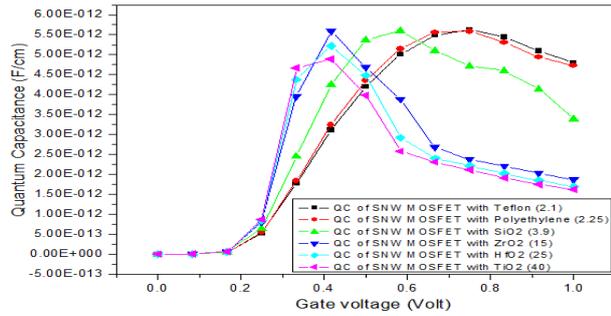Fig.3. (a) Variation in Gate control parameter

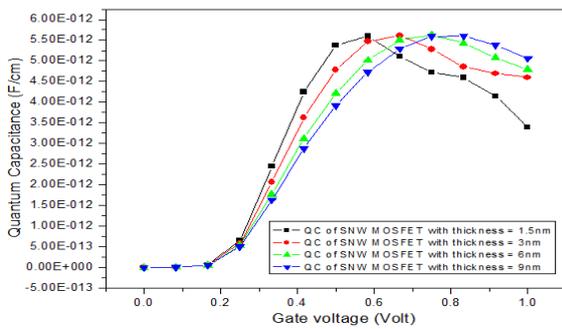Fig.3. (b) Variation in Dielectric material
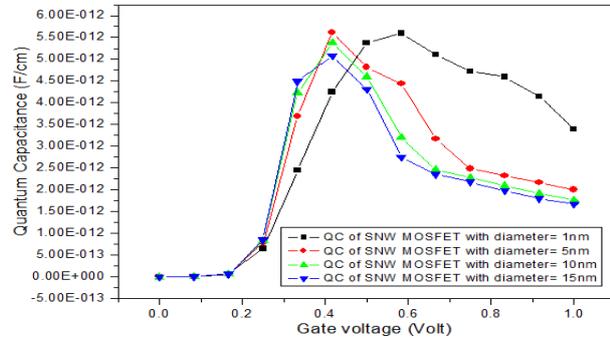

Fig.3. (c) Variation in Dielectric thickness

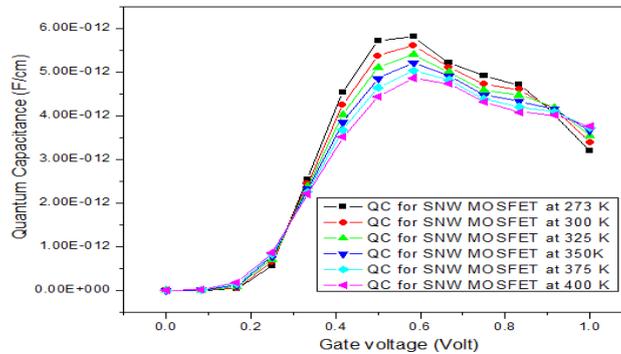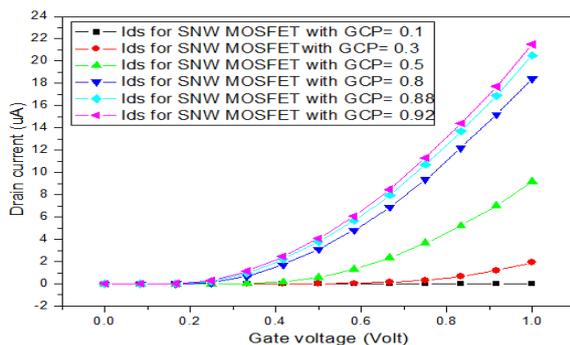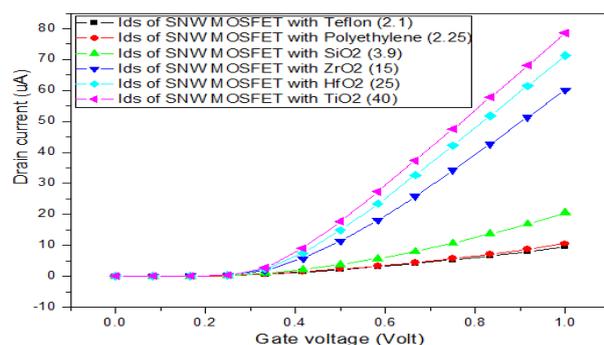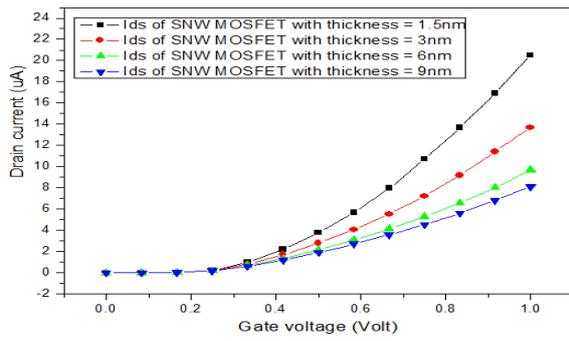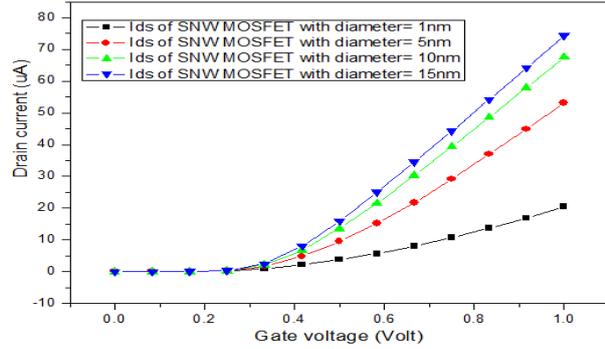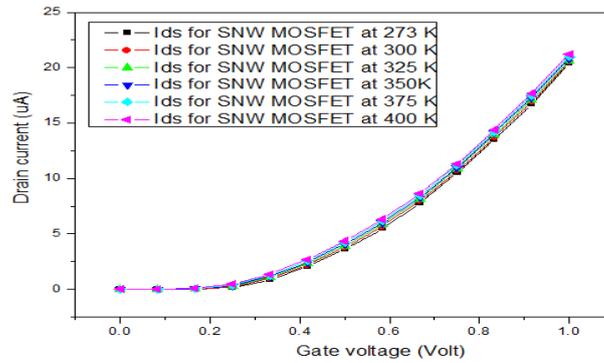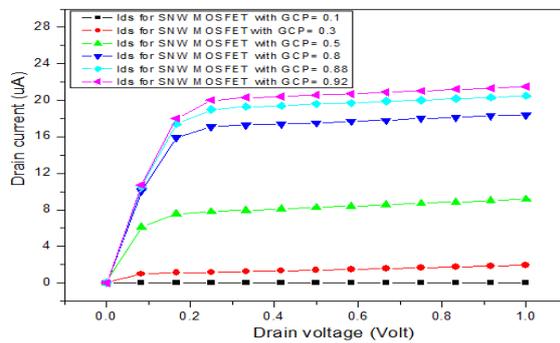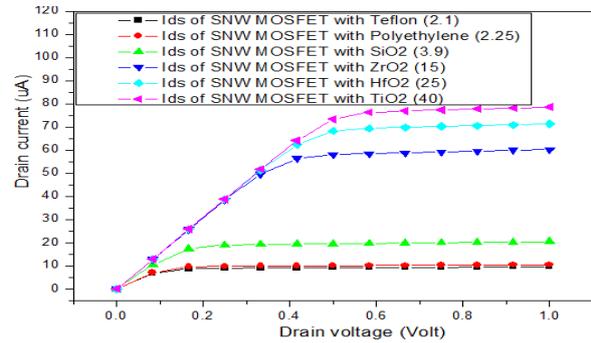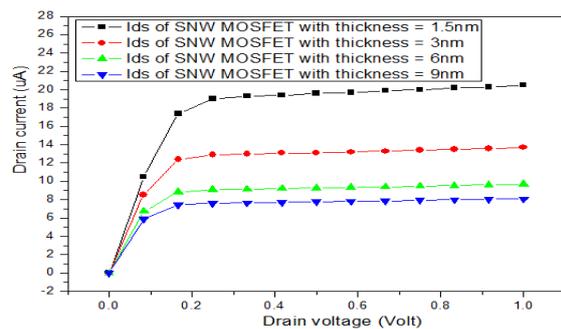Fig.3. (d) Variation in SNW diameter

Fig.3. (e) Variation in temperature

The simulation results shows that Quantum Capacitance decreases with decrease in GCP, high-k dielectric materials, decrease in dielectric thickness, with increase in SNW diameter and with increase in temperature.

3.2. Drain current Vs Gate voltage
Simulations were carried out to obtain Drain current for a sweep in gate voltage (0 to 1V) in a silicon nano wire MOSFET with Drain voltage as 1V and variations in input parameters.

Fig.4. (a) Variation in Gate control parameter

Fig.4. (b) Variation in Dielectric material

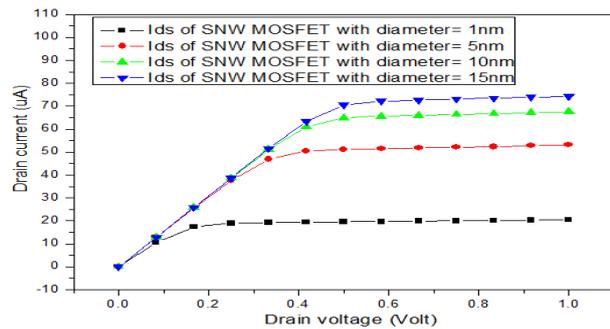Fig.4. (c) Variation in Dielectric thickness

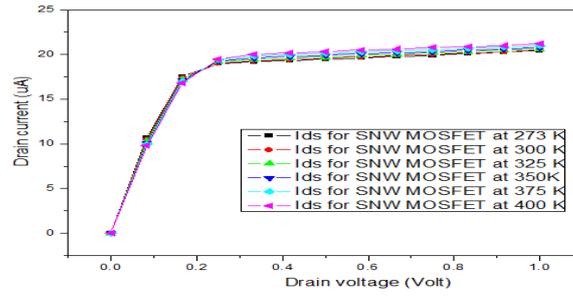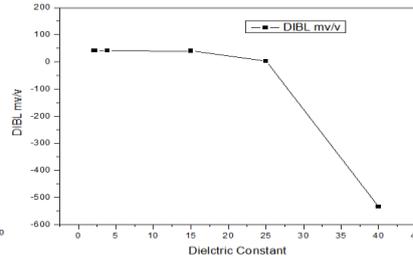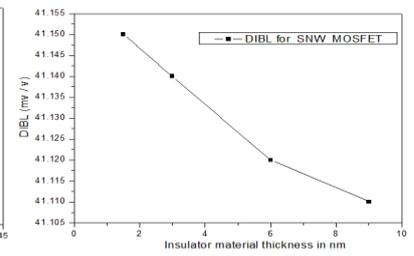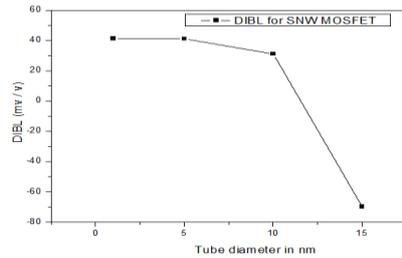

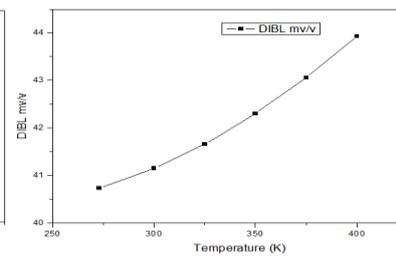Fig.4. (d) Variation in SNW diameter

Fig.4. (e) Variation in temperature

The simulation results shows that the drain current increases with increase in GCP, high-k dielectric materials, with decrease in dielectric thickness, with increase in SNW diameter and there is no appreciable variation for change in temperature.

3.3. Drain current Vs drain voltage

Simulations were carried out to obtain Drain current for a sweep in drain voltage (0 to 1V) in a silicon nano wire MOSFET with Gate voltage as 1V and variations in input parameters as follows

Fig.5. (a) Variation in Gate control parameter
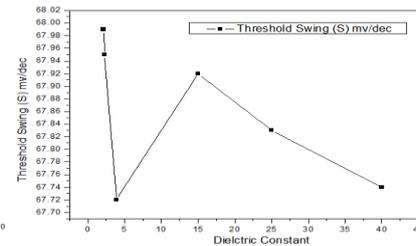

Fig.5. (b) Variation in Dielectric material

Fig.5. (c) Variation in Dielectric thickness

Fig.5. (d) Variation in SNW diameter

Fig.5. (e) Variation in temperature

The simulation results show that the drain current increases with increase in GCP, high-k dielectric materials, with decrease in dielectric thickness, with increase in SNW diameter and there is no appreciable variation for change in temperature.

3.4. Drain Induced Barrier lowering

Simulations were carried out to obtain Drain Induced Barrier lowering in a silicon nano wire MOSFET with gate voltage as 0-1V, drain voltage as 0-1V and variations in input parameters as follows

Fig.6. (a) Variation in GCP

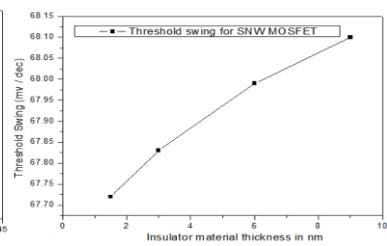Fig.6. (b) Variation in Dielectric material

Fig.6. (c) Variation in Dielectric thickness

Fig.6. (d) Variation in SNW diameter

Fig.6. (e) Variation in temperature

The simulation results shows that the DIBL decreases with increase in GCP, high-k dielectric materials, increase in dielectric thickness, increase in SNW diameter and it increases when increase in temperature.

3.5. Threshold swing

Simulations were carried out to obtain Threshold swing in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters as follows

Fig.7. (a) Variation in GCP

Fig.7. (b) Variation in Dielectric material

Fig.7. (c) Variation in Dielectric thickness
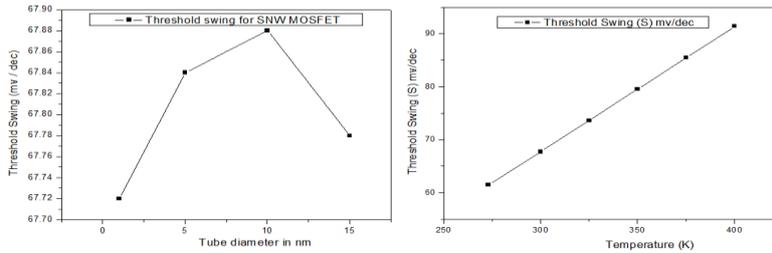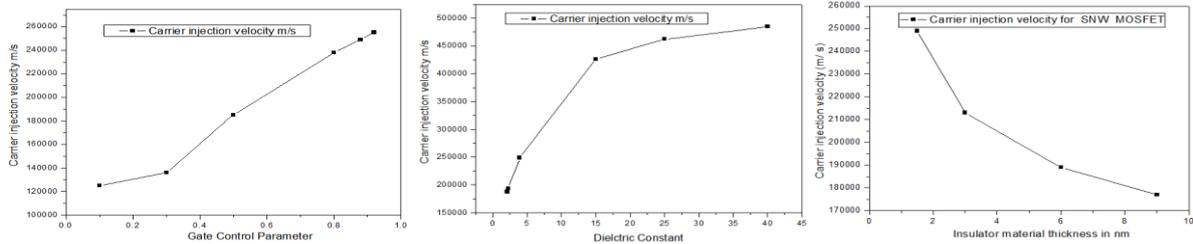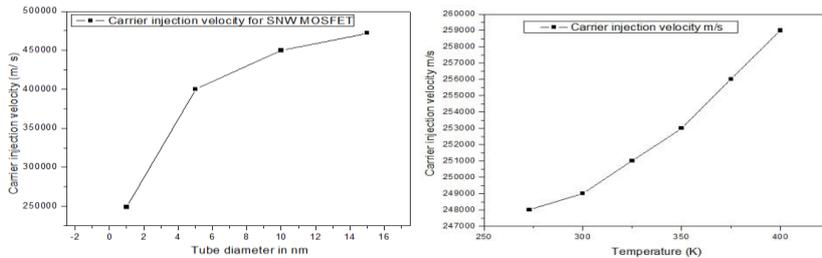
Fig.7. (d) Variation in SNW diameter   Fig.7. (e) Variation in temperature

The simulation results show that threshold swing decreases with increase in GCP and high-k dielectric materials. It increase for increase in dielectric thickness, increase in diameter (upto 10nm), with increase in temperature.

3.6. Carrier injection velocity

Simulations were carried out to obtain carrier injection velocity in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters

Fig.8. (a) Variation in GCP   Fig.8. (b) Variation in Dielectric material   Fig.8. (c) Variation in Dielectric thickness

Fig.8. (d) Variation in SNW diameter   Fig.8. (e) Variation in temperature

The simulation results show that carrier injection velocity increases with increase in GCP, high-k dielectric materials, increase in SNW diameter, increase in temperature and decreases with increase in dielectric thickness.

3.7. On current

Simulations were carried out to obtain on current in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters
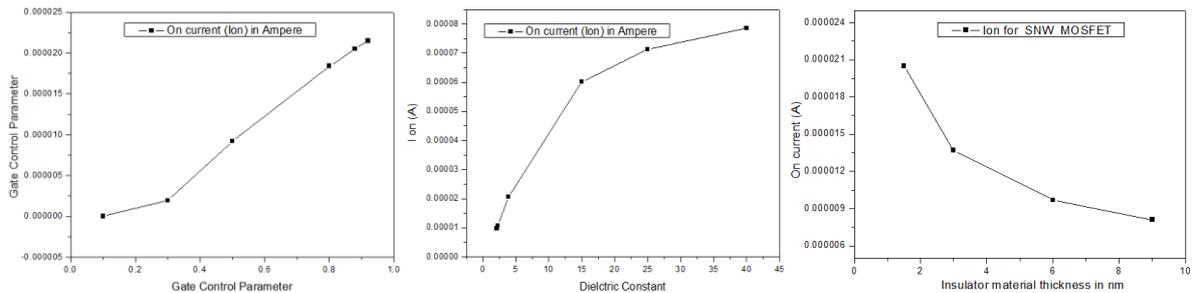

Fig.9. (a) Variation in GCP   Fig.9. (b) Variation in Dielectric material   Fig.9. (c) Variation in Dielectric thickness
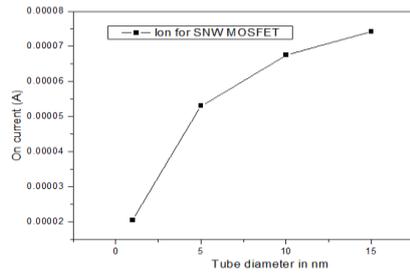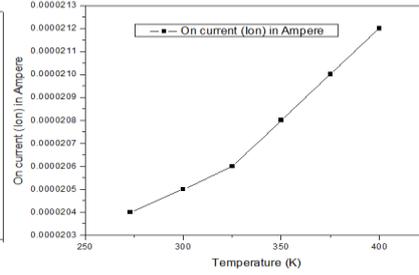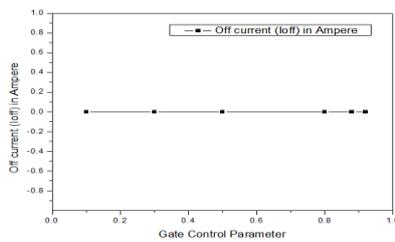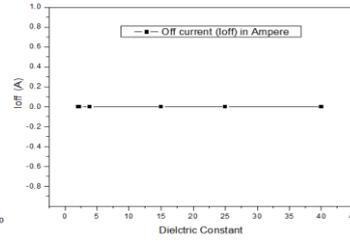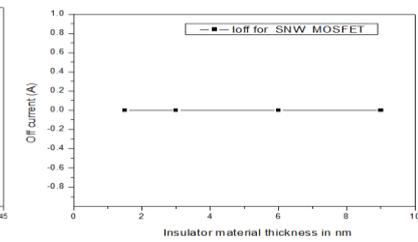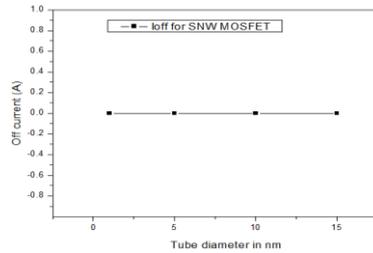
Fig.9. (d) Variation in SNW diameter

Fig.9. (e) Variation in temperature

The simulation results show that On current (I_{on}) increases with increase in GCP, high-k dielectric materials, with increase in SNW diameter, with increase in temperature and decreases with increase in dielectric thickness.

3.8. Off current

Simulations were carried out to obtain off current in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters

Fig.10. (a) Variation in GCP

Fig.10. (b) Variation in Dielectric material

Fig.10. (c) Variation in Dielectric thickness

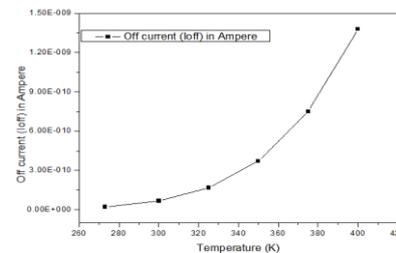

Fig.10. (d) Variation in SNW diameter

Fig.10. (e) Variation in temperature

The simulation results show that off current (I_{off}) increases with increase in temperature and no variation for change in GCP, dielectrics, dielectric thickness and SNW diameter.

3.9. Output conductance

Simulations were carried out to obtain output conductance in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters
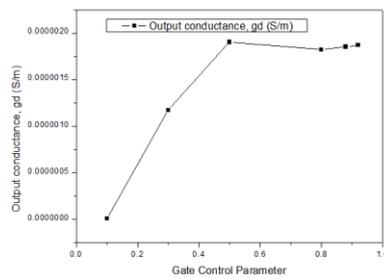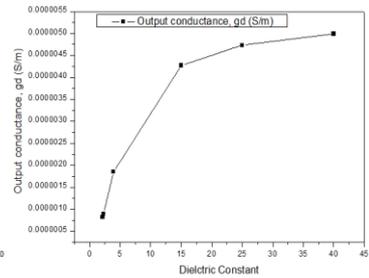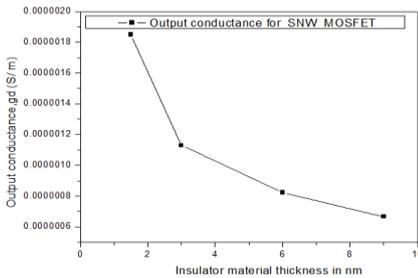

Fig.11. (a) Variation in GCP

Fig.11. (b) Variation in Dielectric material

Fig.11. (c) Variation in Dielectric thickness
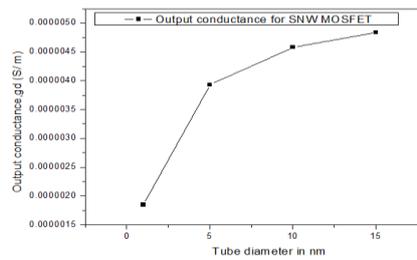
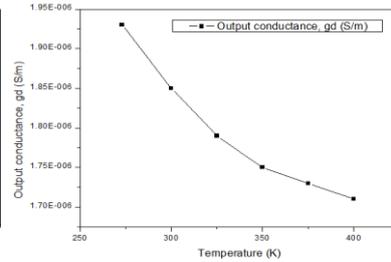Fig.11. (d) Variation in SNW diameter   Fig.11. (e) Variation in temperature

The simulation results show that output conductance increases with increase in GCP, high-k dielectric materials, with increase in SNW diameter and decreases with increase in dielectric thickness, with increase in temperature.

3.10. Transconductance

Simulations were carried out to obtain transconductance in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters
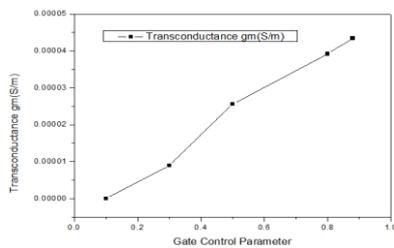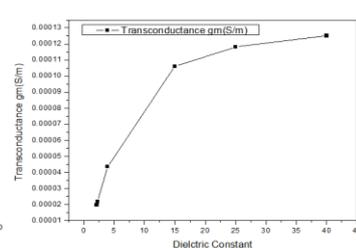

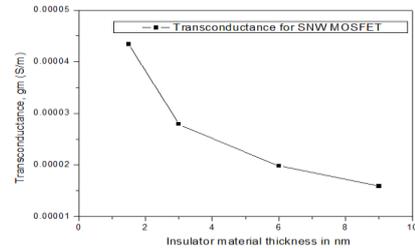Fig.12. (a) Variation in GCP   Fig.12. (b) Variation in Dielectric material   Fig.12. (c) Variation in Dielectric thickness
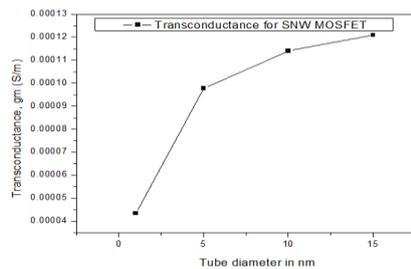

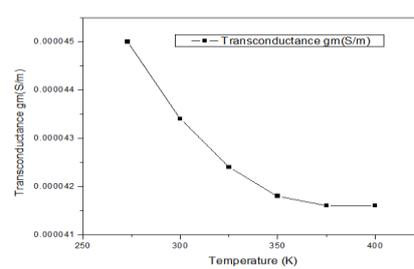Fig.12. (d) Variation in SNW diameter   Fig.12. (e) Variation in temperature

The simulation results show that transconductance increases with increase in GCP, high-k dielectric materials, with increase in SNW diameter and decreases with increase in dielectric thickness, with increase in temperature.

3.11. Voltage gain

Simulations were carried out to obtain voltage gain in a silicon nano wire MOSFET with gate voltage as 0-1V and drain voltage as 0-1V and variations in input parameters
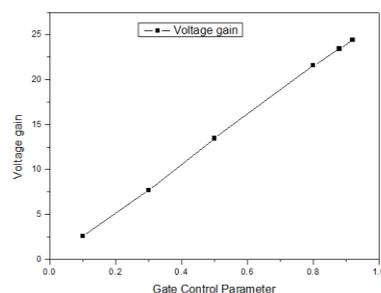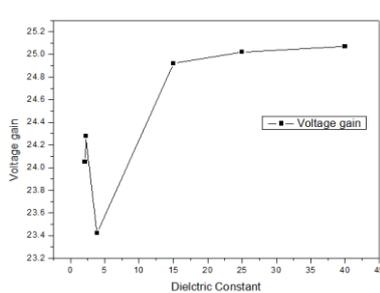

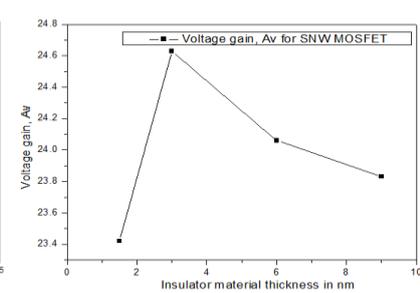Fig.13. (a) Variation in GCP   Fig.13. (b) Variation in Dielectric material   Fig.13. (c) Variation in Dielectric thickness
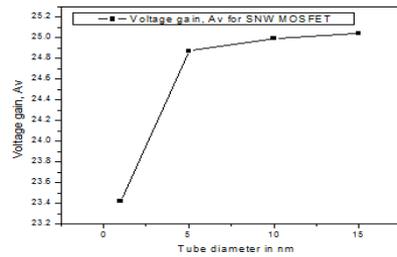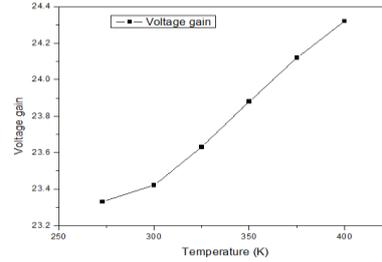
Fig.13. (d) Variation in SNW diameter   Fig.13. (e) Variation in temperature

The simulation results show that voltage gain increases with increase in GCP, high-k dielectric materials, with increase in SNW diameter, with increase in temperature and decreases with increase in dielectric thickness.

IV.   Conclusions

The various output parameters of silicon nanowire MOSFET were studied. From the discussions of the simulation results, we can conclude that in order to have better performance, the various input parameters should be high GCP, High-k dielectric materials, Small dielectric thickness, Large silicon nanowire diameter and low temperature is advisable.

References

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