A Design of RF – Based Programmable Frequency Divider for IEEE 802.11a Wireless Access

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Abstract: *The purpose of my project is to design & simulate the frequency divider using ADS software. My project is totally emphasized on the IEEE 802.11 a standard. The IEEE 802.11a describes the WLAN standard. The basis of the project is the SCL (Source Coupled Logic). This thesis organization provides an overview of the evolution of digitally programmable FREQUENCY DIVIDER using CMOS technology.*
Keywords – *Dual Modulus Prescaler, OFDM, RS Latch, SCL, Swallow Counter.*

I.   Introduction

Frequency being a parameter of the electronic signal give the researchers, a wide scope to improve & standardize the electronics & telecommunication system in the most productive & efficient way. As the telecommunication system is flourishing, it uses frequency as one of the most important parameter for its development. In mobile, Telecommunication, computer communication, division of frequency to perform selection for centre frequency & synthesizing frequency is becoming most important & critical task now-a-days. In Wireless Communications System there is a necessity of different wireless standards for different applications. However, common to almost all of these standards is that the data to be transferred is somehow modulated on a radio frequency (RF) carrier, and the modulated signal is then transmitted over the air, and received and demodulated in the receiving end. In both the transmitting and the receiving end, an accurate RF carrier signal must be generated. Therefore, a radio frequency synthesizer is always required, regardless of the wireless standard.

The frequency divider is an important building block in today's RFIC and microwave circuits because it is an integral part of the phase-locked loop (PLL) circuit. In a typical PLL loop, the output of the voltage-controlled oscillator (VCO) is divided down by the frequency divider to a frequency the temperature-compensated crystal oscillator (TCXO) operates (typically from 10 MHz to 30 MHz). The divided signal and TCXO are fed into the phase detector for comparison. The output phase difference is used to adjust the VCO output frequency. The frequency divider is also widely used to generate a precision I/Q signal if the input signal has a 50% duty cycle, for the modern in-phase and quadrature (I/Q) modulator or demodulator. For the signal with duty cycle other than 50%, an additional divide-by-2 can be used to generate the 50% duty cycle. Compared with the traditional resistor and capacitor (RC) quadrature generation, the frequency divider approach is easier to implement, is lower power and offers smaller phase imbalance.

II.   Source Coupled Logic

SCL gates are differential. The implementation of logic functions is based on the series-gating approach, i.e., by stacking source coupled pairs. However, this approach severely limits the minimum supply voltage allowed for proper operation of stacked transistor pairs, which can be a serious drawback in current low-voltage low-power circuits.

2.1. Topology and Operation

SCL is a dual rail logic circuit that use both the variable and its complement $(A,\bar{A})$ as an input pair. The output of a dual rail circuit is also a pair $(E, \bar{E})$ that drives the next gate(s) in the logic cascade. However, dual rail logic interprets the difference $(E-\bar{E})$ as the logic variable instead of just one or the other. When viewed at the level of Boolean algebra, the use of both the variable and it is complement is superfluous; the result is the same as that found using a single-rail circuit. Moreover, dual rail networks are more complicated to wire.

The circuit schematic of SCL inverter gate, shown in Fig. is made up of an NMOS source-coupled pair having transistors working in the saturation or cut off region, that approximate well the behaviour of a voltage controlled current switch. The biasing current (Iss) is steered to one of the two output branches and converted into a differential output voltage by two PMOS transistor working in the linear region (Active load pull up resistance). The logic function of the SCL is implemented by the logic block connected between the active load (PMOS) and the current source (Iss). For an inverter/buffer, the logic block is the differential pair constructed by NMOS transistors M1 and M2.The SCL gate uses PMOS active load, but other types of load, such as physical resistor or a diode connected NMOS/PMOS could be used. However, resistor load is not normally chosen since

large silicon area needed and its parasitic capacitance can be high. For the second type of load, the output levels will loss the threshold voltage furthermore; the MOS diode load is slower than the PMOS active load for practical bias currents. SCL inverter the operation of the SCL logic is based on the input differential pair circuit. The two inputs control the flow of current through the two branches of the differential pair. For example, if VGS (M2) is higher than VGS (M1), the current ID2 exceeds the current ID1.
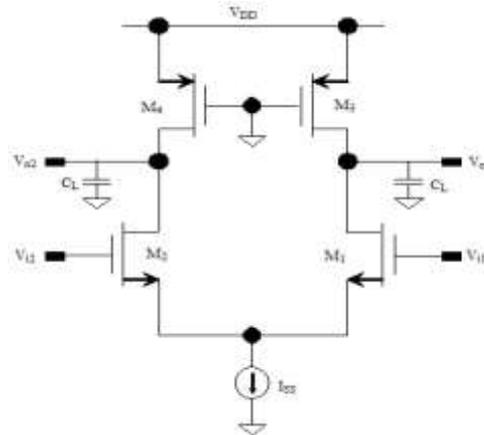
Fig. 1. SCL inverter.

Therefore, the output voltage Vo2 begins to drop until it reach steady sate , where the current going through PMOS active load (M4) matches the ID2. In mean time Vo1 is charged to VDD through M3.The output voltage swing V_{swing} is defined as voltage difference between Vo1 and Vo2 at steady state. The amount of current passing through the ON branch(M2) controls the delay of the logic gate transition $(1 \rightarrow 0)$, while the PMOS active load (M3) controls the charging of the output nodes $(0 \rightarrow 1$ transition). Defining, ΔV as the voltage drop of M3 (M4) due to the drain current equal to Iss, the logic swing of the gate, V_{swing} equals $2\Delta V$. To achieve best performance, all current must pass through the ON branch and the load resistance (PMOS) should be small in order to reduce the RC delay.

The SCL has several advantages. The primary benefit of using SCL over other types of logic is speed. Circuits implementing with SCL logic can operate at higher frequencies. SCL circuits are also ideal for integration into low noise environments, due to their differential nature and lack of switching noise.
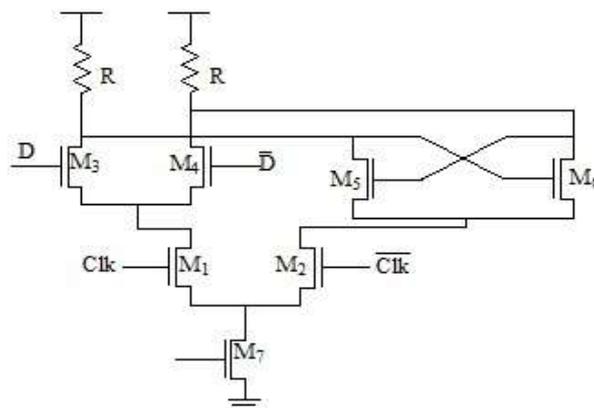

Fig. 2. Schematic of an SCL D latch.

III. Orthogonal Frequency – Division Multiplexing

Orthogonal frequency-division multiplexing (OFDM), essentially identical to coded OFDM (COFDM) and discrete multi-tone modulation (DMT), is a frequency-division multiplexing (FDM) scheme utilized as a digital multi-carrier modulation method. A large number of closely-spaced orthogonal sub-carriers are used to carry data. The data is divided into several parallel data streams or channels, one for each sub-carrier. Each subcarrier is modulated with a conventional modulation scheme (such as quadrature amplitude modulation or phase-shift keying) at a low symbol rate, maintaining total data rates similar to conventional single-carrier modulation schemes in the same bandwidth. OFDM has developed into a popular scheme for wideband digital

communication, whether wireless or over copper wires, used in applications such as digital television and audio broadcasting, wireless networking and broadband internet access.

The primary advantage of OFDM over single-carrier schemes is its ability to cope with severe channel conditions (for example, attenuation of high frequencies in a long copper wire, narrowband interference and frequency-selective fading due to multipath) without complex equalization filters. Channel equalization is simplified because OFDM may be viewed as using many slowly-modulated narrowband signals rather than one rapidly modulated wideband signal. OFDM prove robustness in multi-path propagation environment. Due to the use of many sub-carriers, OFDM is more tolerant of delay spread.

The operating bands and channels of OFDM are given below:

Band	Channel numbers	Frequency (MHz)	Maximum output power (up to 6 dB antenna gain)
U – NII lower band 95.15 to 5.25 MHz	36	5180	40 mW (2.5 mW/MHZ)
	40	5200	
	44	5220	
	48	5240	
U – NII lower band 95.15 to 5.25 MHz	52	5260	200 mW (12.5 mW/MHz)
	56	5280	
	60	5300	
	64	5320	

IV.   IEEE 802.11

The IEEE 802.11 specification (ISO/IEC 8802-11) is an international standard describing the characteristics of a wireless local area network (WLAN). The 802.11 standard reserves the low levels of the OSI model for a wireless connection that uses electromagnetic waves. The physical layer defines the radio wave modulation and signalling characteristics for data transmission, while the data link layer defines the interface between the machine's bus and the physical layer, in particular an access method close to the one used in the Ethernet standard and rules for communication between the stations of the network.

The 802.11a standard has a maximum theoretical data flow of 54 Mbps, five times that of 802.11b, but at a range of only about thirty metres. The 802.11a standard relies on a technology called OFDM (Orthogonal Frequency Division Multiplexing). It broadcasts in the 5 GHz frequency range and uses 8 non-overlapping channels.

In this layer the frequency ranges are divided into 3 bands, namely 5.15GHz – 5.25GHz as lower band, 5.25GHz – 5.35GHz as middle band and finally 5.725GHz – 5.825GHz as upper band. The FCC has licensed 12 channels for 802.11a. These channels are spaced at 20MHz apart. Though they are considered non-interfering, they do have a little overlap in the frequency spectrum. So it is recommended when possible to separate adjacent cell channels by at least 1 channel.
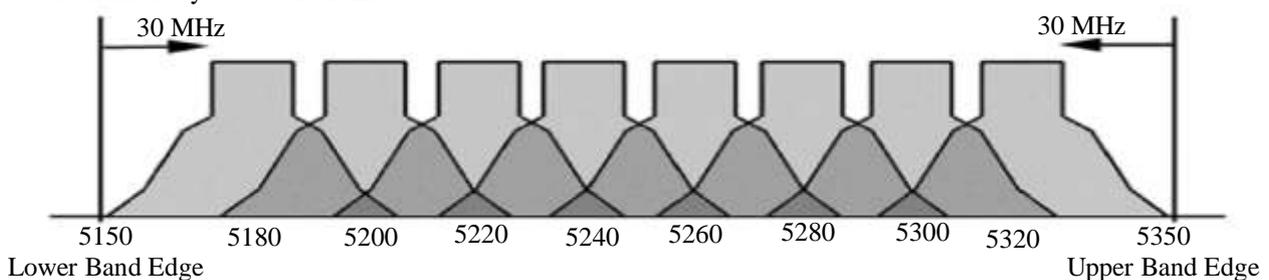

Fig. 3. 802.11a channel in lower and upper U – NII bands.

3.   UNII Channelization

There are three main unlicensed-spectrum frequency bands suitable for sophisticated data transmission. The industrial, scientific, and medical (ISM) bands in the United States include 900 MHz, 2.4 GHz, and 5.8 GHz. The unlicensed national information structure (U-NII) and high performance radio local-area networks (HiperLAN2) bands are in the 5 GHz band.

3.1. Channel Numbering

The channel numbering system is dependent on the centre frequency. The centre frequency is the geometric mean between lower cut off frequency & upper cut off frequency of a frequency band. Channel centre

frequencies are defined at every integral multiple of 5 MHz above 5 GHz. The relationship between centre frequency and channel number is given by the following equation:

Channel centre frequency = $5000 + 5 \times N_{ch}$ (1)

Where Nch = 0, 1 … 200; and denotes the channel numbers.

When the channels frequencies are 5180, 5200, 5220, 5240, 5260, 5280, 5300, and 5320 etc. then the numbers of channels are 36, 40, 44, 48, 52, 56, 60, and 64 respectively.

This definition provides a unique numbering system for all channels with 5 MHz spacing from 5 GHz to 6 GHz, as well as the flexibility to define channelization sets for all current and future regulatory domains.

V. Frequency Divider

The programmable frequency divider is the core module of the frequency synthesizer. The divider is based on a pulse-swallow topology. It's a conventional implementation, consisting of a N/N+1 prescaler (dual-modulus prescaler), a fixed-ratio program counter, and a programmable swallow counter. The RS latch is typically included in the swallow counter and is drawn explicitly here for clarity. The prescaler begins the operation by dividing by N+ 1 until the swallow counter is full. The RS latch is then set, changing the prescaler modulus to N and disabling the swallow counter. The division continues until the program counter is full and the RS latch is reset. The overall divide ratio is therefore equal to NP + S, where N is the prescaler, P is fixed ratio program counter & S is the channel selection bit in binary format.
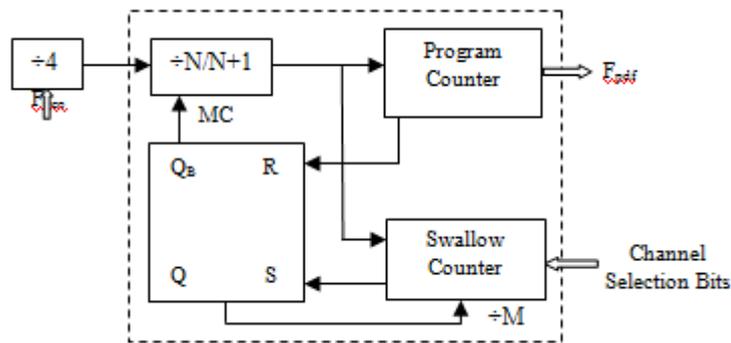

Fig. 4. Programable Frequency Divider.

A critical decision in the design of the divider is the choice between low-swing current-steering logic and rail-to-rail CMOS logic. Simulations of the circuit with various values of N, P, S indicate that the minimum power dissipation occurs if the prescaler incorporates current steering, its output is converted to rail-to-rail swings, and the remainder of the circuit incorporates standard dynamic and static CMOS logic. The use of current steering in the prescaler also obviates the need for large oscillator swings, saving power in the VCO buffer.

VI. Elements of Frequency Divider

3.2. Prescaler

A prescaler is an important building block in a PLL, where it divides the VCO frequency to a lower frequency before the phase detector.

Within the frequency divider, the prescaler is the block that operates at a higher frequency and therefore consumes more power. Conventionally, prescaler have been implemented using a high frequency synchronous divider, in which the D-flip-flops of the synchronous dividers are running at the highest frequency, significantly increasing the clock load and the power consumption. Even worse, these synchronous dividers have logic gates in the critical path, introducing additional delays and causing a reduction in the maximum operating frequency.

Design and operation of some basic prescalers are given below:

3.2.1. ÷ 2 Prescaler

A Johnson counter is an easy and popular implementation of a ÷2 prescaler. Two D latches are coupled in a loop, and clocked by inverse clocks. When 'IN' goes low the signal at OUT bar is being transferred to the output of the first D-latch, and transferred further to the OUT when 'IN' goes high again. The timing diagram shows that OUT inverts every time 'IN' goes high, so time division is doubled and thus frequency is divided by two.
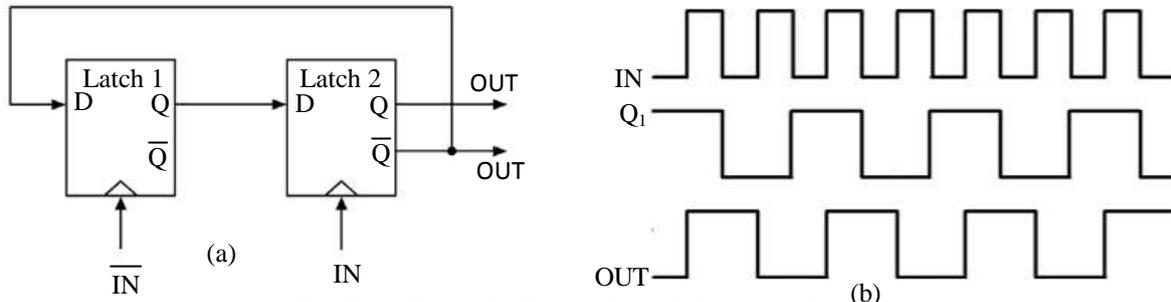
Fig. 5. (a) Divide by 2 prescaler and (b) timing diagram.

3.2.2. ÷ 3 Prescaler

The ÷3 circuit is utilizing two D-latch and an AND gate. Both flip-flops are being clocked by the rising edge of 'IN'. When 'IN' goes high the signal at OU Tbar is being transferred to the input of the AND gate and transferred further to the OUT of the second D-latch. It is seen from the timing diagram that the time division is multiplied by 3, and thus frequency is divided by three.
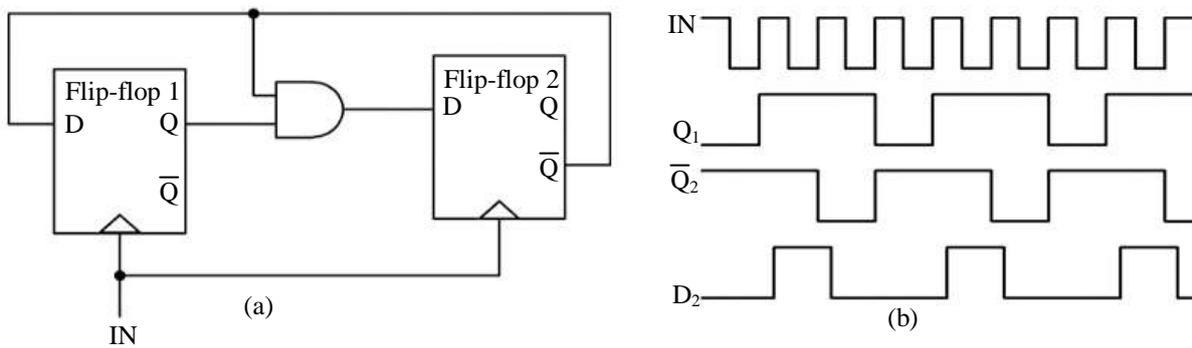

Fig. 6. (a) Divide by 3 prescaler and (b) timing diagram.

3.2.3. ÷ 2/3 Prescaler

The prescaler consists of two D-latches, one AND gate & one OR gate. The circuit divides the frequency of the input signal by either 2 or 3, depending on the logic state of the modulus control signal M. When M is low the output of the OR gate will be controlled directly by Q1, and the circuit will operate in the same way as the ÷3 circuit.

When M is set high the output of the OR gate will be high independent of the output of the first flip-flop. Thus the output of the AND gate follows Q2bar. On every rising edge of 'IN' Q2bar will be inverted and thus the frequency is divided by 2.
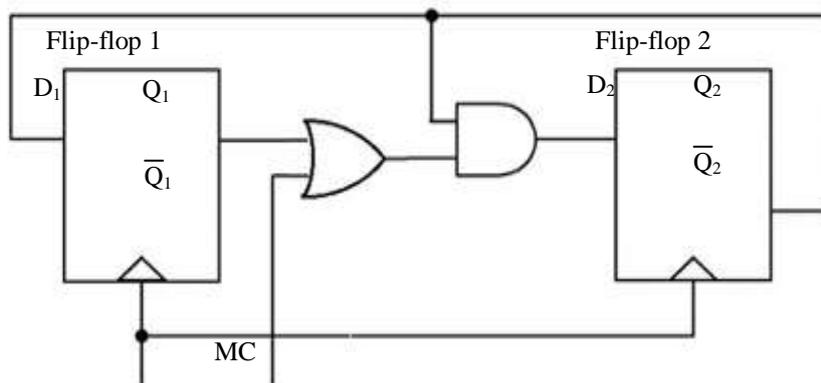

Fig. 7. 2 by 3 prescaler.

3.2.4. 16/17 Dual Modulus Prescaler

The architecture of the required 16/17 dual modulus prescaler is shown in figure. The 16/17 prescaler circuit consists of a 2/3 dual modulus prescaler and three numbers of divide by 2 circuits. As already mentioned when MC = 0 this will divide the input frequency by 17 and when MC = 1 frequency will be divided by 16. The final

output of this prescaler is given as input to the program counter, and shallow counter. Actually it's the prescalar using which we have completed our project successfully.
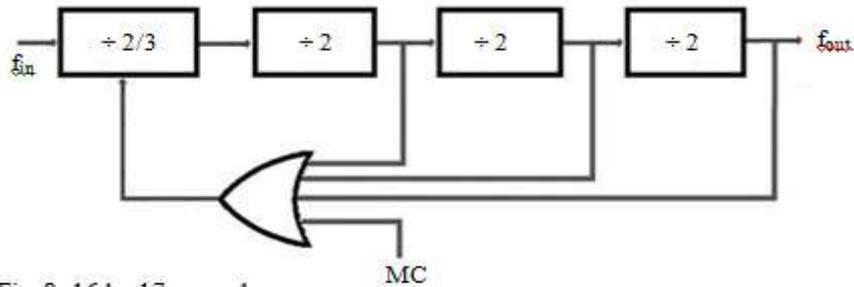

Fig. 8. 16 by 17 prescaler.

3.3. Program Counter

The design consists of four numbers of $\div 2$ circuit and three NAND gates. Here four D – flip – flops are connected in cascading manner with output of one flip – flop given as input to the other flip – flop and the output of each FF are given as input to the NAND gates. And finally, the output of the third NAND gate is given as reset input to the SR – Latch. If reset is high modulus control signal M = 1. For this program counter the inputs are given from the output of 16/17 prescaler.
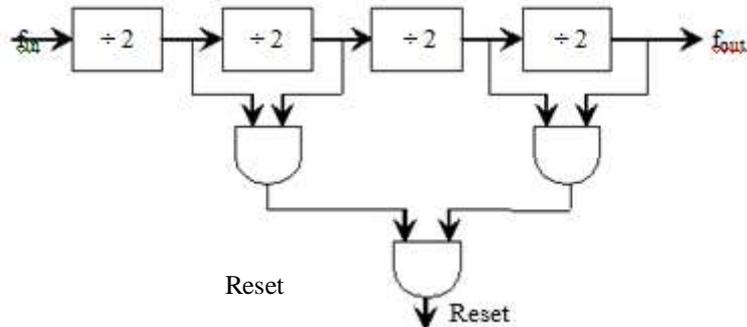
Fig. 9. The designed circuit for program counter.

3.4. Swallow Counter

The Swallow Counter is one of the three building blocks (swallow counter, main counter, and dual-modulus prescaler) that constitute the programmable divider commonly used in modern frequency synthesizers. The swallow counter is used to control the dual modulus prescaler which is set to either N or (N+1). At the initial reset state, the prescaler is set to a divide ratio of (N+1), but the swallow counter will change this divide ratio to N when it finishes counting S number of cycles.

The frequency divider consists of a N/N+1 prescaler followed by a program and shallow counter. The program counter generates one output pulse for every P input pulses. The Swallow Counter gets its name from the idea that it "swallows" 1 from (N+1) of the dual-modulus prescaler. The swallow counter is used to control the dual-modulus prescaler which is set to either N or (N+1).
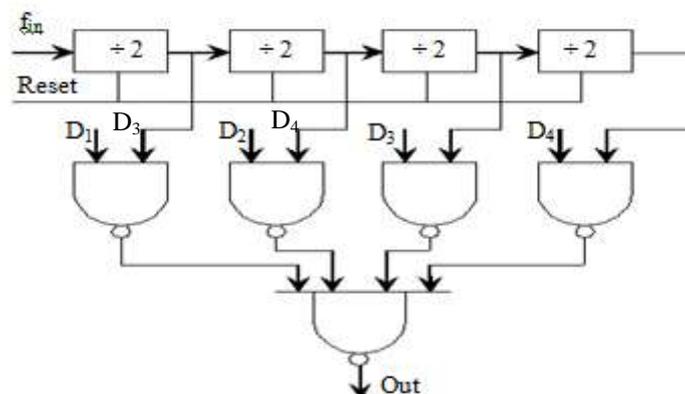

Fig. 10. Block diagram of a swallow counter.

In shallow counter design eight D flip-flop with reset input are connected in cascade manner. Here also output of one F-F is given as input to other F-F and each outputs of the entire FF are given as inputs to the NAND gate as shown in schematic in figure above. The other inputs to the NAND gates are the controlling inputs i.e. channel selection inputs in binary format. The output of the swallow counter goes to the reset of the SR latch. The output of the program counter goes to the set of the SR latch. So the output of the SR latch is 0 and then MC=0.

3.4.1. Division Ratio

At the beginning of the cycle modulus control signal M = 0 and the prescaler divides frequency by (N + 1). After s cycles, with S determined by the channel selection bits, M is set to 1 and the prescaler divides by N for the rest of the cycle. Therefore the overall division ratio is:

$$M = (N + 1) S + N (P - S)$$
$$\text{Or, } M = NP + S \tag{2}$$

Where N is prescaler, P is fixed ratio program counter and S is channel selection bit in binary format. Considering f_{ref} = 5 MHz, f_{in}/f_{ref} = M and by choosing N = P = 16, if S = 3, 4, 5, 6, 7, 8, 9, 10 etc. then f_{in} = 5180 MHz, 5200 MHz, 5220 MHz, 5240 MHz, 5260 MHz, 5280 MHz, 5300 MHz, 5320 MHz respectively.

3.5. SR Latch

A bi-stable SR flip-flop or SR latch is activated or set by logic "1" applied to its S input and deactivated or reset by a logic "1" applied to its R. The SR flip-flop is said to be in an "invalid" condition (Meta-stable) if both the set and reset inputs are activated simultaneously.
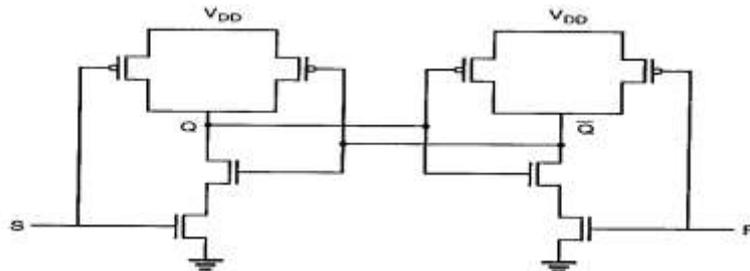

Fig. 11. SR latch designed by CMOS logic.

In my project, SET input of SR Latch is driven by the output of the Swallow Counter and RESET input of the latch is driven by the output of the Program Counter. The output of the latch is used as the Modulus Control signal, which controls the operation of the prescalar section.

VII.   Simulation Results
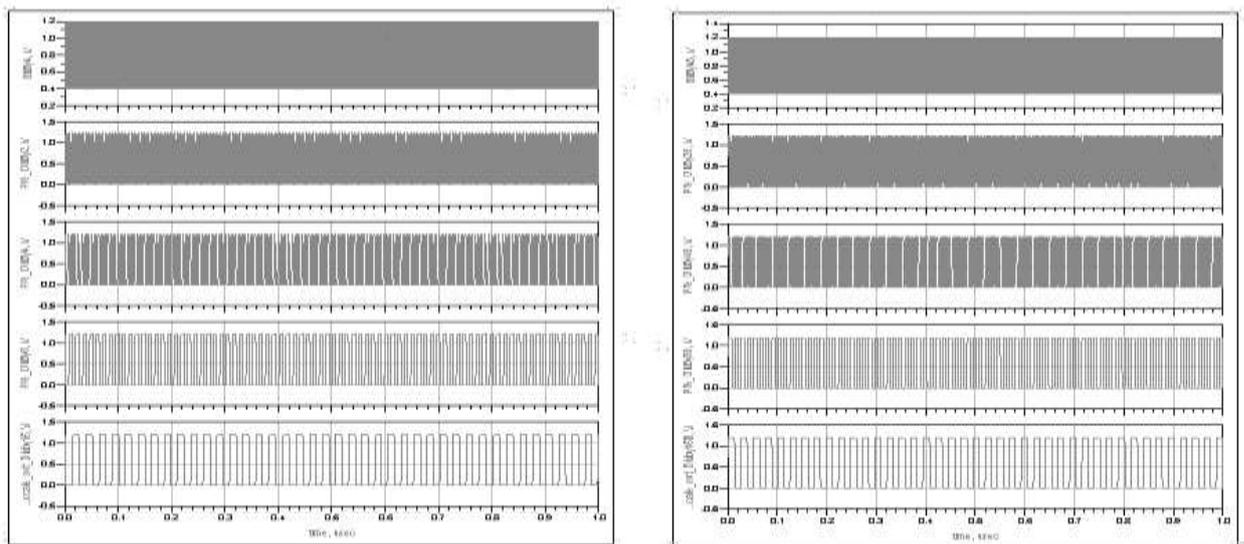### 3.6. Simulation Results of 16/17 Prescaler
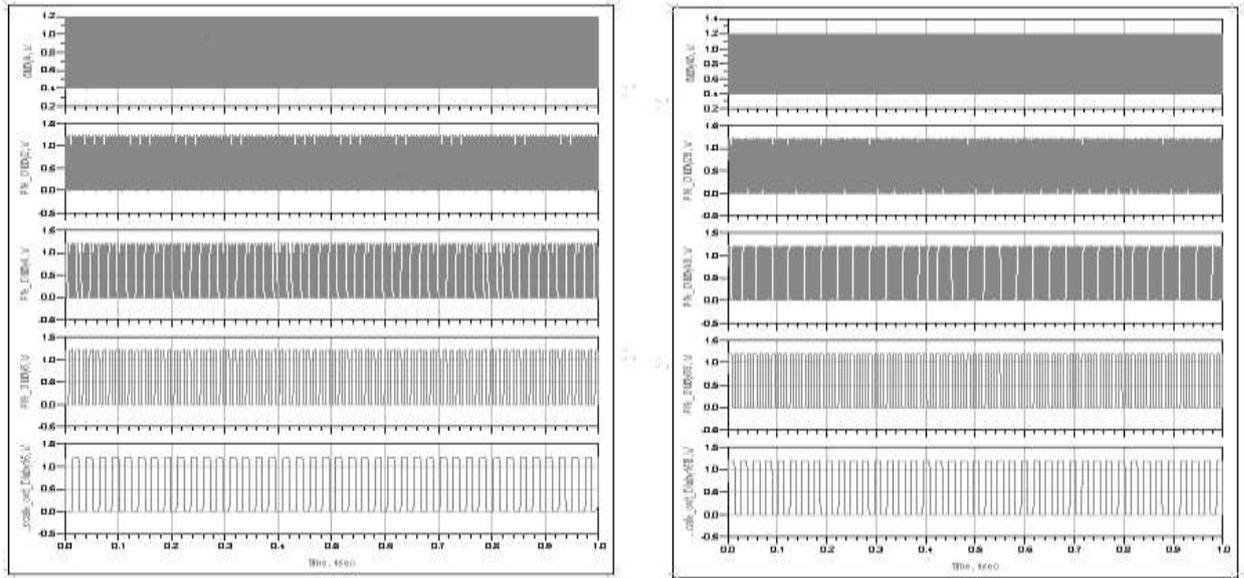

Fig. 12. Simulation at 5.24 GHz.

Fig. 13. Simulation at 5.30 GHz.

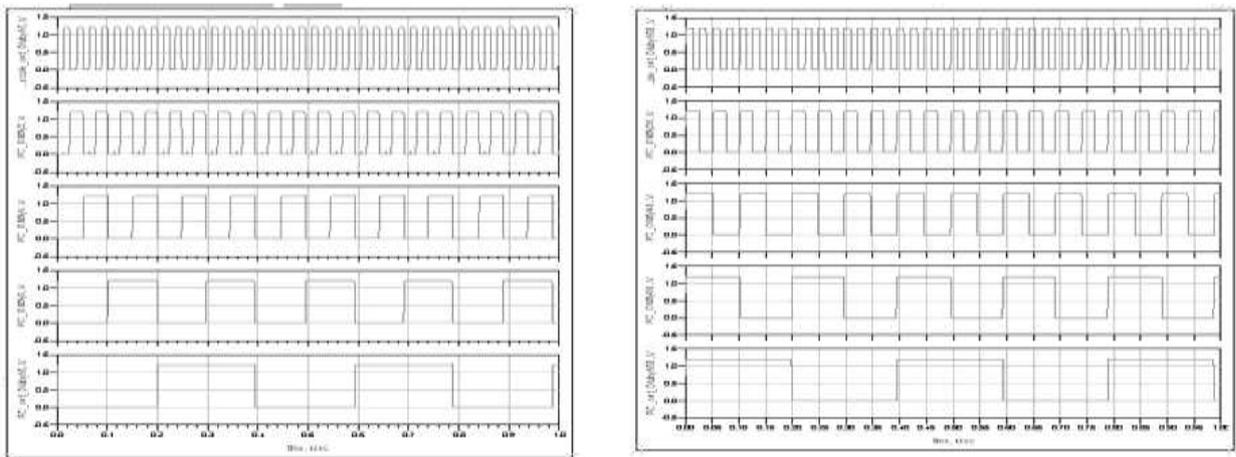### 3.7. Simulation Results of Program Counter
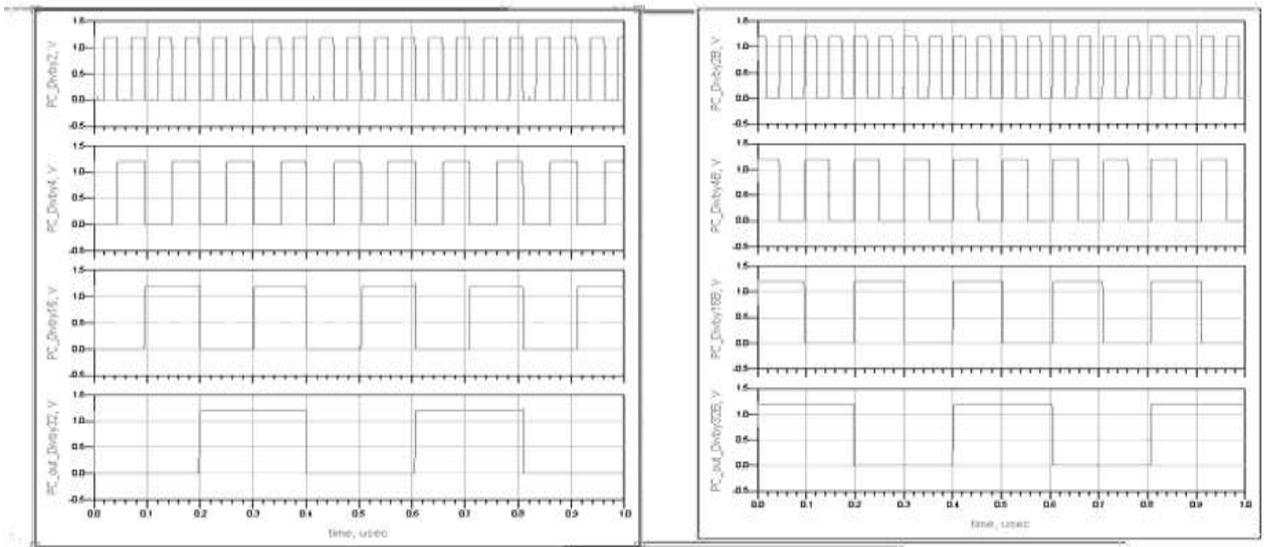

Fig. 14. Simulation at 5.24 GHz.

Fig. 15. Simulation at 5.30 GHz.

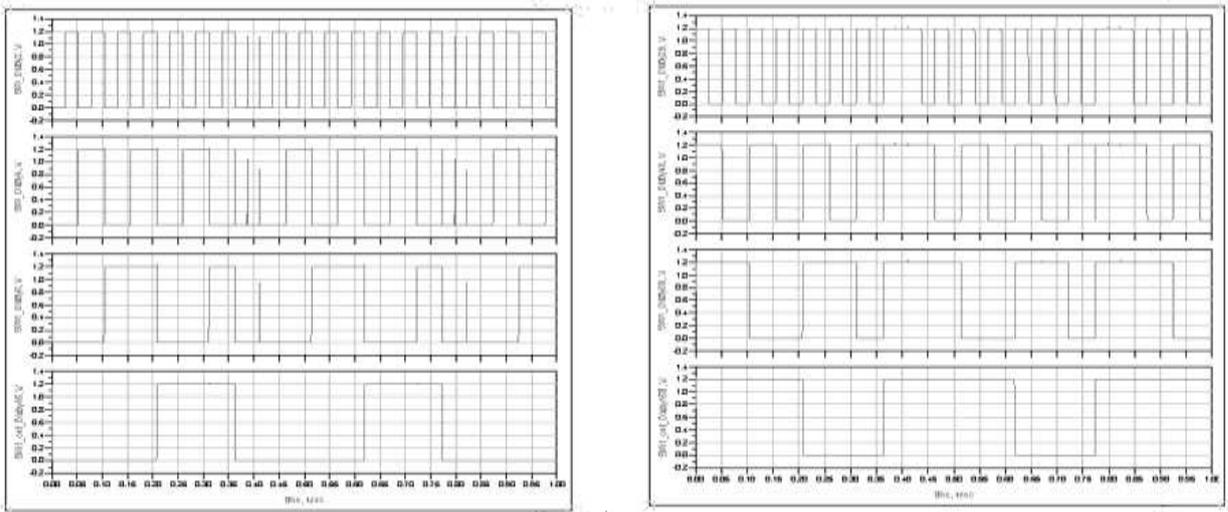**3.8. Simulation Results of Swallow Counter**
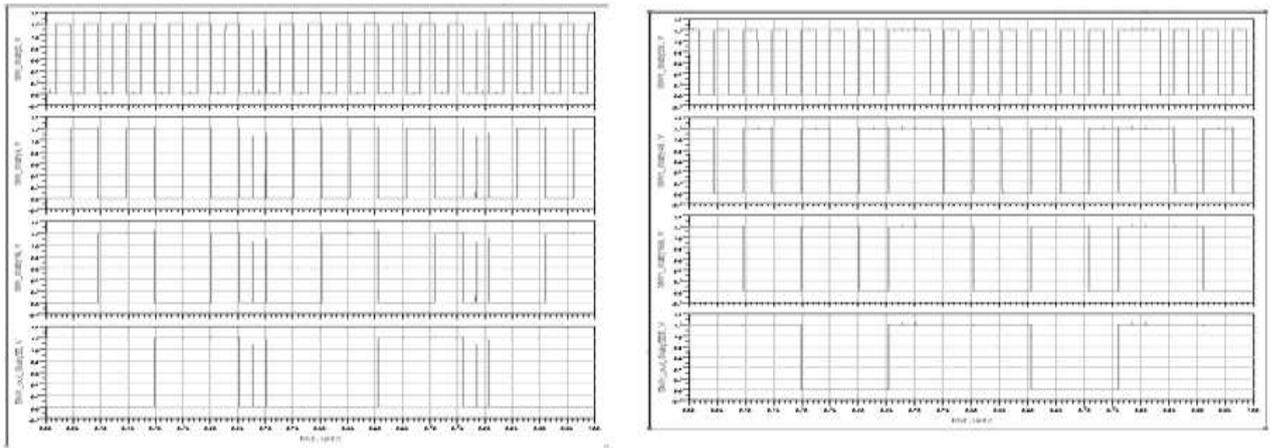

Fig. 16. Simulation at 5.24 GHz.

Fig. 17. Simulation at 5.30 GHz.

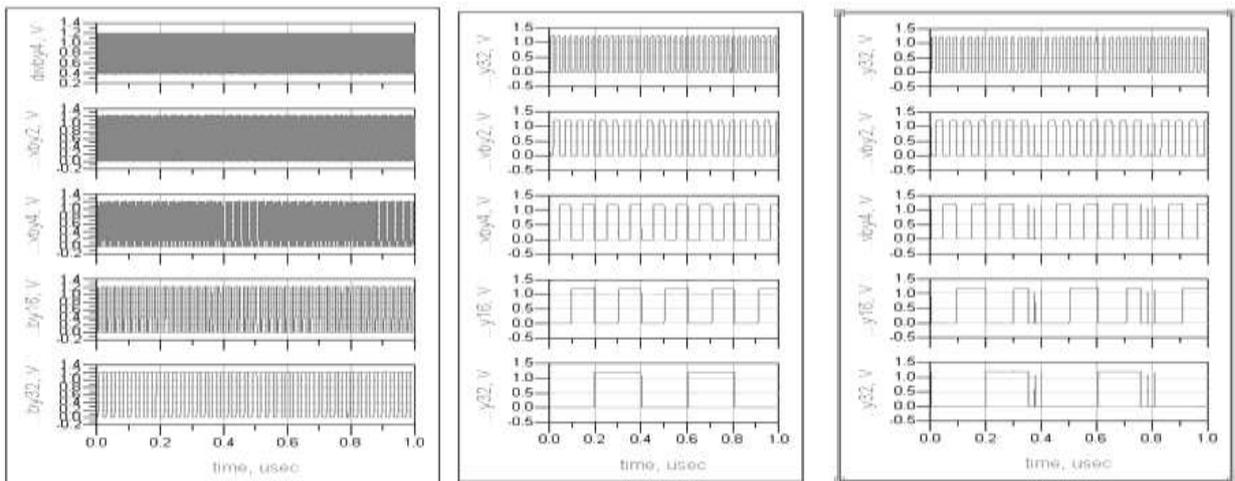**3.9.   Simulation Results of Frequency Divider**
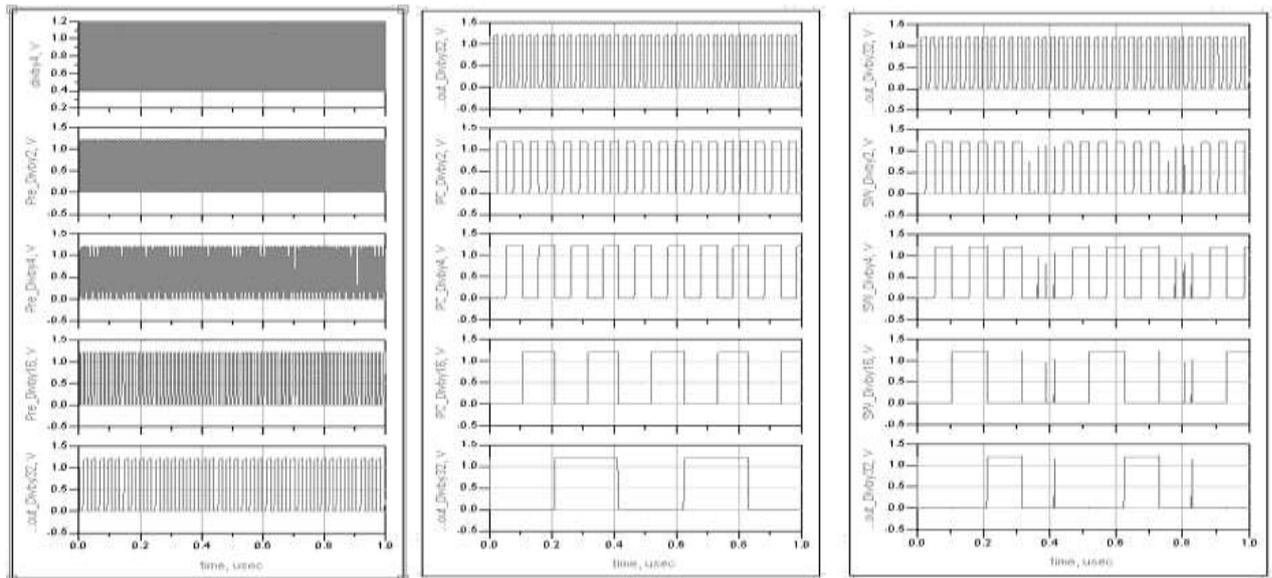

Fig. 18. Simulation at 5.24 GHz.

Fig. 19. Simulation at 5.30 GHz.

VIII.   Conclusion

This dissertation has presented a general overview of short range wireless communication standards. A DFF capable of high speed operation is described. A good noise performance compared to other published circuits is achieved while operating at a high frequency from a low supply voltage. A multi-modulus prescaler, able to divide by any integer modulus in the range 64 to 127, has been designed. Program counter & Swallow counter are designed using 16/17 prescaler. A RS latch is designed using CMOS technology. Simulated results of all the designed circuit are obtained at different centre frequencies of IEEE 802.11a WLAN. The required output at each step of any designed circuit can be understood, by seeing the results. A high-speed programmable divider operating at a low supply voltage is presented. Particular emphasis was placed in the study and analysis of a key building block of frequency divider. At last, after designing the whole divider circuit using 16/17 prescaler and providing the channel selection bit 'S' all the centre frequencies of lower band & middle band of IEEE 802.11a WLAN are generated. Simulation results of centre frequencies of 5.24 GHz and 5.30 GHz are only shown here.

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