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Behavioral Design and Synthesis of 64 BIT ALU using Xilinx ISE

Rajib Chetia, Kaushik Chandra Deva Sarma, Gaurab Baruah
(Asst. Professor, CIT, Kokrajhar) (Asst. Professor, CIT, Kokrajhar)
(M.Tech student .in ECT, Gauhati University)

Abstract: *This paper presents the behavioral Design and synthesis of a 64 bit ALU. 64 bit ALU is basically a multiplexer that operates mainly 16 operations as per select line Bit-permutation. Flags are other important indicators used for specific purpose e.g. if Sign Flag is HIGH then the output of ALU must be a negative number. CLR can reset the output of ALU.*
Keywords: *Flags, CLR, 64 Bit ALU, VHDL.*

I. Introduction

VHDL is used as the specification and synthesis language, but the process of transformation is substantially more automated. Specifically, the process of High-level simulation is maintained by the transformation from the level of description into hardware elements being automated. With the Synthesis route, the process of mapping into particular targeted circuit technologies is automated (e.g. Spartan 6E) .The Synthesis process therefore both increases productivity (through automation) and reduces flexibility (by restricting the choice of technology.

II. Behavioral Modeling

The Behavioral Style architecture contains concurrent statements with sections of sequential statements that describe the outputs of the circuit at a discrete moment in time given particular inputs. While similar language constructs are often found in Dataflow and Behavioral style architectures, only the latter explicitly exhibit the notions of time and control. This style describes the functions of the circuit at the algorithmic level. The highest level of abstraction is the behavioral level that describes a system in terms of what it does (or how it behaves) rather than in terms of its components and interconnection between them

III. ALU Operations:

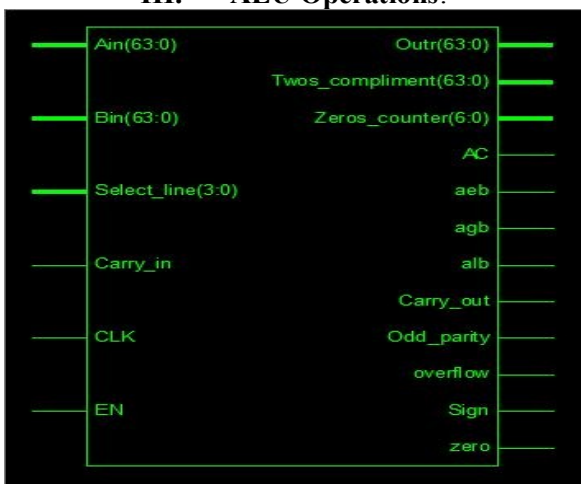

Fig.1.1: Entity 64 Bit ALU

3.1 Arithmetic Operations

Carry Look Ahead Adder is a faster adder that overcomes the delay of Ripple Carry Adder. ALU can operate addition; subtraction etc. between Ain and Bin input bus.

3.2 Logic operations

All basic logic operations are included e.g. XOR, NAND, NOR, AND etc.

3.3 Flags Status

Flags are too much important in HDL Designing of ALU. All Flags like Sign, Overflow, Carry, Parity, Auxiliary Carry, and Zero. Flags actually allow us to determine the result of an operation more efficiently e.g. Overflow Flag shows occurrence of overflow condition during an operation.

3.4 Comparator

ALU compares the inputs Ain and Bin and results whether Ain>Bin, Ain=Bin or Ain<Bin.

3.5 Others

Enable, CLR are other parameters that are used to control the operations of ALU. CLR resets the output to logic 0. If Enable is set to logic 1 the ALU retains the value stored from previous clock cycle.

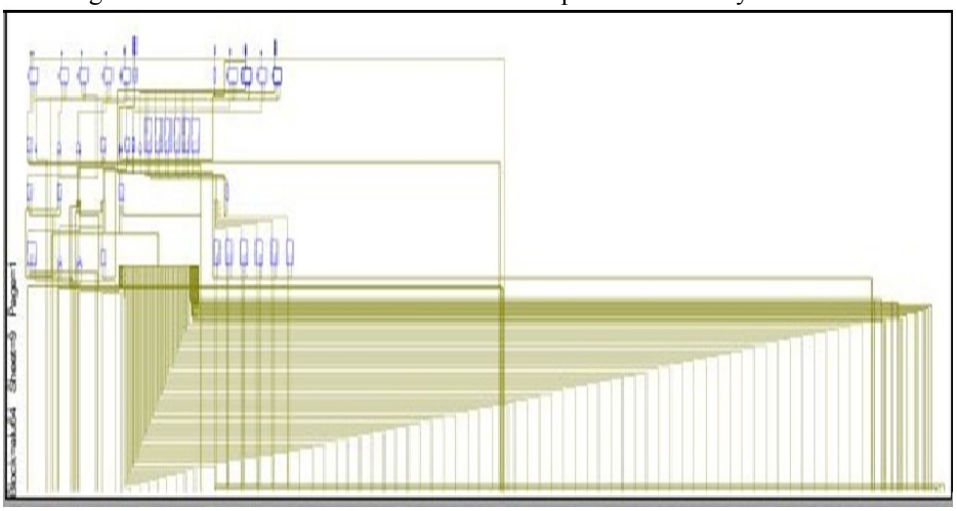

Fig. 1.2: RTL Schematic.

Table 1:

SELECT LINE	OPERATION	SELECT LINE	OPERATION
0000	Ain AND Bin	1000	Ain XNOR Bin
0001	Ain OR Bin	1001	NOT (Ain NAND Bin)
0010	Ain and (NOT Bin)	1010	NOT (Ain NOR Bin)
0011	NOT Ain	1011	Carry Ripple Adder, Carry, Overflow
0100	NOT Bin	1100	Carry Ripple Adder, Carry, Overflow
0101	Ain NAND Bin	1101	64 Bit Adder
0110	Ain NOR Bin	1110	64 Bit Subtractor
0111	Ain XOR Bin	1111	Ain NOR (NOT Bin)

IV. Xilinx Simulation:

Simulation of 64 Bit ALU for the Behavioral model has been performed for 1000 nano-seconds (ns). Each Clock cycle has 100 ns rise time and 100 ns fall time. The simulation of 64 Bit ALU(if rising_edge(CLK) and EN=0) generated from Testbench Waveform is given in figure 2.1 and 2.2 below.

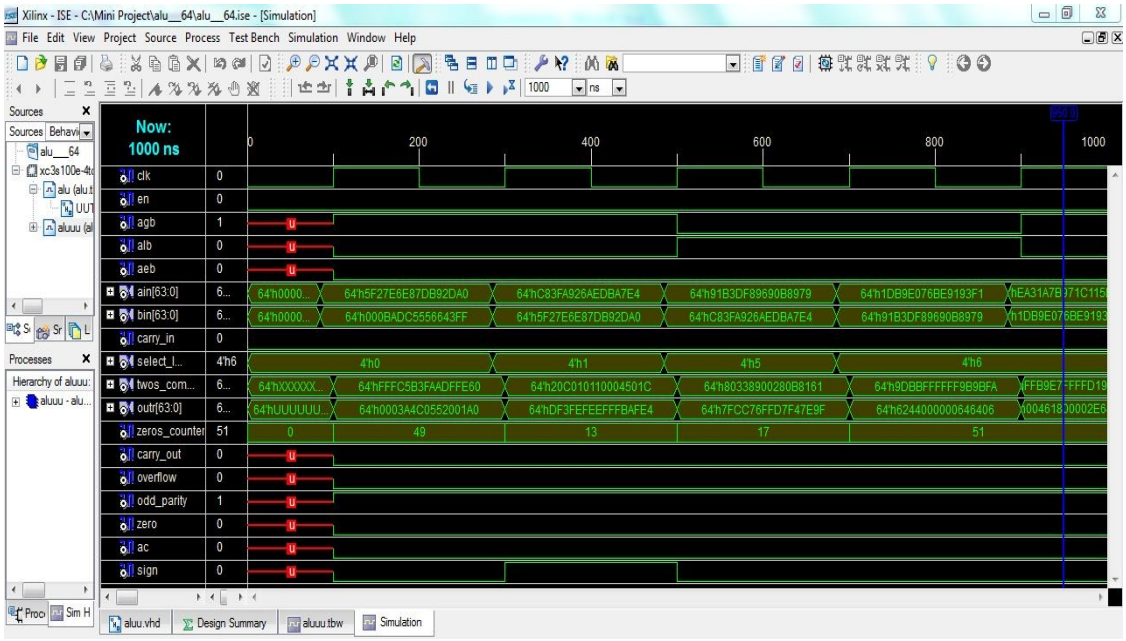

Figure 2.1: Testbench Simulation.

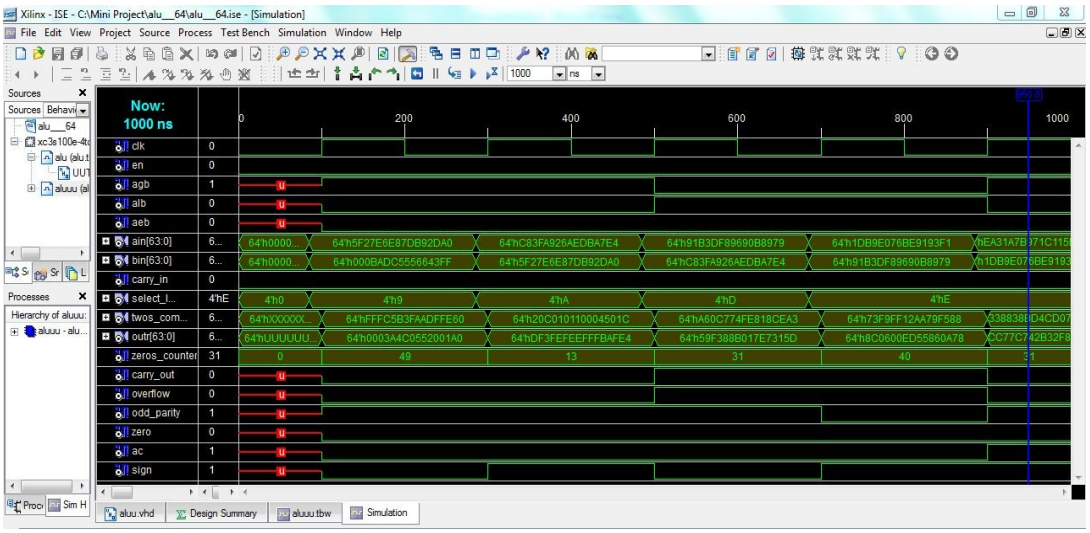

Figure 2.2: Testbench Simulation

V. Synthesis and Implementation Report:

Xilinx-ISE v9.1i has generated the Synthesis and Implementation report for the behavioral model of 64 Bit ALU and are given below:

```
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 67
 1-bit adder carry out                                 : 1
 2-bit adder                                           : 1
 2-bit adder carry out                                 : 1
 3-bit adder                                           : 3
 3-bit adder carry out                                 : 1
 4-bit adder                                           : 7
 4-bit adder carry out                                 : 1
 5-bit adder                                           : 15
 5-bit adder carry out                                 : 1
 6-bit adder                                           : 31
 6-bit adder carry out                                 : 1
 64-bit adder                                          : 1
 65-bit adder                                          : 1
 65-bit adder carry in                                 : 1
 65-bit subtractor                                     : 1
# Registers                                            : 78
 Flip-Flops                                            : 78
# Comparators                                          : 3
 64-bit comparator equal                               : 1
 64-bit comparator greater                             : 1
 64-bit comparator less                                : 1
# Multiplexers                                         : 4
 1-bit 16-to-1 multiplexer                             : 3
 64-bit 16-to-1 multiplexer                            : 1
# Xors                                                 : 70
 1-bit xor2                                            : 3
 1-bit xor3                                            : 65
 1-bit xor64                                           : 1
 64-bit xor2                                           : 1

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.054ns (Maximum Frequency: 486.855MHz)
   Minimum input arrival time before clock: 94.949ns
   Maximum output required time after clock: 10.535ns
   Maximum combinational path delay: No path found
```

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	857	960	89%
Number of Slice Flip Flops	65	1920	3%
Number of 4 input LUTs	1521	1920	79%
Number of bonded IOBs	279	108	258%
Number of GCLKs	1	24	4%

Figure 3: Design Utilization Summary.

VI. Conclusion:

The 64 bit ALU is designed and synthesized using Xilinx ise v9.1i and targeted to Spartan device. The ALU is a major component of the CPU(Central Processing Unit). It performs arithmetic computation such as Addition, Subtraction, Comparator, Overflow and all basic logical operations (AND, OR, NOT, NOR, XOR, XNOR, NAND). We have verified the results obtained from Xilinx ISE Design Suit v9.1i with the theoretical results for all the operations that were performed and found that they match with the theoretical values.

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