III-V MOSFET ALTERNATIVE TO Si/SiO$_2$ MOSFET

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ABSTRACT : *Silicon planar MOSFET's are approaching their scaling limits. Major challenges in MOSFET scaling are the "short channel effects" which limits the MOSFET performance. As MOSFET's shrink in dimensions, the source and drain regions move closer to each other & reducing device performance due to Drain Induced Barrier Lowering(DIBL). Hence there is need of alternative device. Among the possible new device designs are DGFET's, FinFET's, Tri-Gate FET's etc. But the III-V MOSFET stands out as one of the most promising MOSFET design due to its maximum gate effect in controlling the short channel effects. In this paper we have explored the III-V MOSFET to replace the currently planar MOSFET's. We have simulate MOSFET by using III-V compound materials like Inp and high-k dielectric material Al2O3.Next phase we find out electrical characteristics (Id-Vd) using device simulator ATLAS.*

Keywords - Al2O3, InP

I. INTRODUCTION

The MOSFET is the basic building block for very large scale integration (VLSI) circuit but due to scaling in MOSFET, short channel effect arises and degrades the device performance. Due to that new device are being explored to replace the existing planner technology. Two types of scaling mechanisms are commonly used, known as constant voltage scaling and constant electric field scaling. Constant voltage scaling is purely geometric approach where the power supply is kept constant and the transistor dimension is scale down. In constant field scaling approach, it involves reducing the transistor dimensions along with power voltage supply in order to maintain the electric field strength in channel.
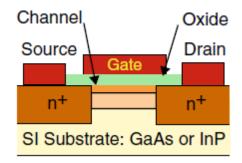
   In long channel device, the source and drain regions are far apart and sufficiently separated that their depletion regions have no effect on potential. In the central region under the gate.

   In MOSFET's there is no any physical contact present in between source & drain. Hence gate parameter plays very essential role in controlling the whole mechanism of MOSFET's. The conduction of current from source to drain starts when we apply sufficient voltage to gate terminal. As MOSFET's are approaching their scaling limits, so to fabricate nanodevices on chip we require another component & new method.

   Now this is the world of nanotechnology & nanodevices fabrication in each field hence III-V MOSFET's plays very significant role in future ultra small CMOS devices. As MOSFET's having its own ability to decrease off leakage current & its structure is very compact & easily understandable to new circuit designers.

II. THEORETICAL APPROACH

 Among all III-V MOSFET represent a promising alternative architecture to the conventional Si technology for devices because of its improved electrostatic control of the channel via gate voltage and consequent suppression of short channel effect. Here InP compound semiconductor is use for InP mosfet and also use high-k material i.e. Al2O3.

Fig. 1 InP MOSFET

In this paper ,we report on simulating n-channel MOSFET on semi-insulating InP substrate with high-k Al2O3.Although InP is a commonly used compound semiconductor with wide applications in electronic, optoelectronic, and photonic devices, high-k dielectric integration on InP is largely unexplored. Compared to GaAs, InP is widely believed to be a more forgiving material with respect to Fermi level pinning and has a higher electron saturation velocity (2×107 cm/s) as well. Detailed Monte-Carlo simulations of deeply scaled n-MOS devices indicate that an InP channel could enable high-field transconductance ~60% higher than either Si, Ge, or GaAs at equivalent channel length .It could be a viable material for high-speed logic applications if a high-quality, thermodynamically stable high-k dielectric could be found. In the few reported works on InP MOSFETs since the 1980s, SiO$_2$ was primarily used as gate dielectric and devices suffered from significant current and threshold voltage drift due to the poor semiconductor-dielectric interface16, 17. Although Fermi-level unpinning was achieved through application of appropriate surface treatment before SiO2 deposition, current and effective channel mobility remained low and interface trap density was far from applicable18–21. By implementing ALD high-k dielectrics on InP, we are able to revisit this historically unsolved problem and demonstrate Fermi-level unpinning of InP surface with ALD high-k dielectrics. InP having higher electron mobility, it gives higher driving current. The advantage of semi-insulating substrate is channel thickness is precisely controlled.

III. DEVICE SIMULATION

Numerical simulation based on Silvaco ATLAS is used to explore the design parameter space for InP MOSFET. Device structure is generated by following step.
1. Mesh formation (auto meshing using   command)
2. Define material
3. Doping profile.
4. Model
5. Numerical method
6. Solution AC and DC
    Using the simulation methodology illustrated in the above section, we simulated InP MOSFET using ATLAS.

IV. RESULT AND DISCUSSIONS

    The device structure of InP MOSFET which simulated using ATLAS having gate length 1μm and gate width 100nm.Here high-k Al2O3 is used as gate dielectric. The gate dielectric having thickness 30nm.P-type substrate is doped with 1×1017cm-3 and source and drain is selectively implant with Si doses of 1×1021cm-3.
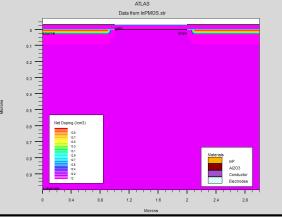

Fig. 2 Device Structure

The fig.2 above shows complete device structure of InP MOSFET which is generated by device simulator ATLAS.
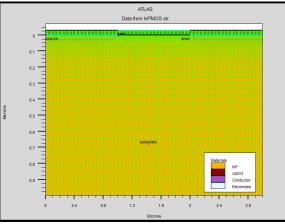
Fig.3 Mesh Structure

The fig.3 above shows mesh structure of InP MOSFET. Meshing is technique to divided computation region into finite submicron so that we can discretize the partial differential equation in this domain to form approximate algebraic system. Mesh quality decide convergence speed .more dense mesh should have more accuracy. We can use dense mesh use in junction region, source and drain.
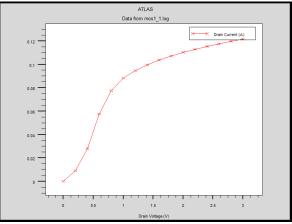

Fig.4 Id-Vd curve at 1V Vgs

Simulated DC output characteristics of InP MOSFET shown in fig.4. Drain current (ID) versus drain bias (VDS) as a function of gate bias (VGS) for Al2O3 (30nm) /InP NMOSFETs with 1-μm gate length. The maximum drain current is 0.12 A/mm at 3V drain bias and 1V gate bias.

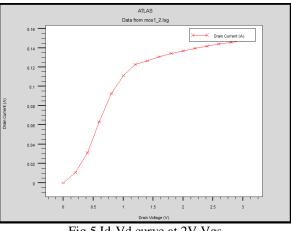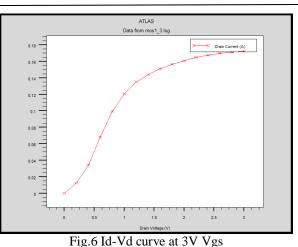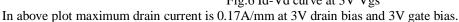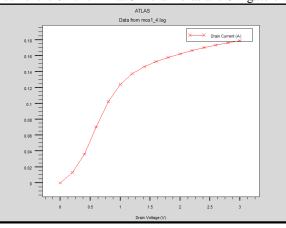Id-Vd curve at 2V, 3V, 4V gate bias as shown in below figure.

Fig.5 Id-Vd curve at 2V Vgs

In above plot maximum drain current is 0.15A/mm at 3V drain bias and 2V gate bias.

Fig.6 Id-Vd curve at 3V Vgs

In above plot maximum drain current is 0.17A/mm at 3V drain bias and 3V gate bias.

Fig.7 Id-Vd curve at 4V Vgs

In above plot maximum drain current is 0.18A/mm at 3V drain bias and 4V gate bias.
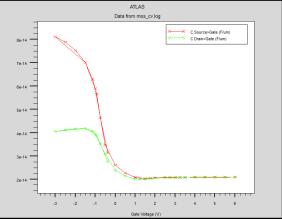

Fig.8 High frequency C-V curve

C-V measurements of metal-oxide semiconductor   capacitors are also carried out to evaluate the interface quality of ALD Al2O3 on InP. 30 nm thick Al2O3 is deposited on a P-type InP substrate at 300 °C by ALD. Frequency is 1MHZ.

V. CONCLUSION

Here we simulate InP MOSFET using atlas device simulator tool and got plot for mesh and device structure. With the help of IV data obtain after simulation we plotted I-V and C-V characteristic

From the above results, we conclude that, the maximum drain current of InP MOSFET is 0.18A/m at 4V gate bias. Complete device structure of InP MOSFET obtained from ATLAS device simulator. This shows InP MOSFET could be the best option for conventional CMOS devices for low power and high speed devices.

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