A Review of Sensor Nodes in Basic Wireless Sensor Networks with an emphasis on processor selection for these networks.

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Abstract: Wireless sensor networks are network of compact micro sensors with wireless communication capability. These sensors have been made viable by convergence of micro-electro-mechanical system (MEMS) technologies and digital electronics. As autonomous devices, they can provide pervasive distributed and collaborative network of computer nodes. There is a wide variety of applications of wireless sensor networks at domestic and industrial level. The factors influencing the design of the sensor networks such as energy resources and power consumption are needed to be taken under consideration. In the design of sensor networks, embedded systems provide a hardware and software platform to interact with environment and other nodes. Networking and power management of wireless is thus important and a current topic of research. This paper deals with the basic concept of wireless communication with respect to the sensor nodes, the factors influencing sensor network.

Keywords: MEMS, Processor, Sensor Nodes, Topology, Wireless Network.

I. Introduction

The recent advances in MEMS has enabled to develop low power, low-cost, multifunctioning sensor nodes that are small in size and communicate untethered over short distances. The integrated low power sensing devices, embedded processes, communication kits and power equipment enable to develop the design of sensor nodes. A sensor network is composed of a large number of sensor nodes, which are densely developed either inside a particular embedded system or with respect to microprocessor. A sensor network represents a significant improvement over traditional sensors. The sensor nodes are supposed to have a few characteristic features so that they can be employed in a wireless network. The factors influencing the design of a sensor network range from fault tolerance, scalability, production costs to power consumption. The choice of processor depends on its architecture which comprises of wake up time, clock scaling, memory architecture, input/output issues etc. Based on these very factors, the sensor nodes are employed in wireless networks to have a widespread domain of its applications. The sensor nodes show a cooperative functioning and thus can be fitted on to a processor board. Instead of sending the raw data to the nodes responsible for functioning, sensor nodes use their processing abilities to locally carry out simple computations and transmit only the required data. The basic diagram of a sensor node is given in Fig 1 below.

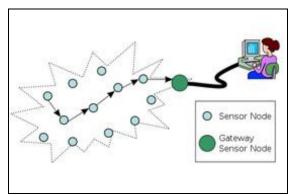


Figure 1. Diagram of a basic sensor node

II. Design of a sensor node

During the design of sensor nodes for wireless sensor networks, few of the characteristics are to be taken care of for better functioning of the network. Theses sensor nodes have to be energy efficient to prevent charging of each node every time. They have to be cost efficient to maintain the budget. Distributed sensing and distributed processing is to be employed in order to deploy more data and process local data using filtering and data fusion algorithms from environment and aggregate this data, transforming it to information. One of the

important features of sensor nodes is its low power consumption. The various factors [1] influencing the design of sensor networks can be categorized under the following:

- a) Fault Tolerance
- b) Scalability
- c) Production Costs
- d) Pre, Post and Development Phases
- e) Re Development Phase
- f) Power Consumptions

Fault tolerance is the ability to sustain sensor network functionalities without any interruption due to a particular sensor node failure. The fault tolerance of a sensor node is modeled using poisson distribution to capture the probability of not having a failure within the time interval $\{t,0\}$.(1)

: $R_k{t}=exp{-l_kt}$ (1) where l_k is the failure rate of sensor node k and t is the time period of the sensor node.

The network for wireless sensor is much huge and it requires many a hundreds or thousands of sensors and sensor nodes. Thus the deploying of sensor nodes may be in a number of hundreds. Depending on the application of wireless sensor networks, the number varies. New techniques must be developed to utilize the high density of the sensor networks. The density can be calculated by (2).

: μ {R}={N π R²} /A (2) where N=number of scattered sensors in region A, R=radio transmission range and μ {R} gives the number of nodes within the transmission radius.

Since the sensor networks consist of a large number of sensor nodes, the cost of a single node is very important to justify the overall cost of sensor network. If the cost of the network is more expensive then deploying traditional sensors, then the sensor network is not cost justified. As a result, the cost of each sensor node has to be kept low. The state of the art technology allows a Bluetooth radio system to be less than 10\$ and the cost of a Pico node has been minimized to less than 1\$.

There are different types of topologies used for the sensor nodes. Few of the basic topologies are given in figure 2. The failure of the nodes makes the topologies useless and hence maintenance is a challenging task. The issues related to the maintenance of topologies is examined in the three basic phases: pre, post and redevelopment phase.

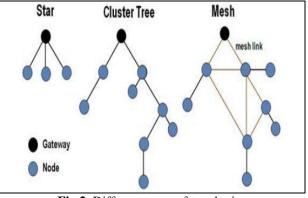


Fig 2. Different types of topologies

The sensor node is made up of four basic components: sensing unit, processing unit, transceiver unit and power unit. Figure 3 shows the components of a sensor node.

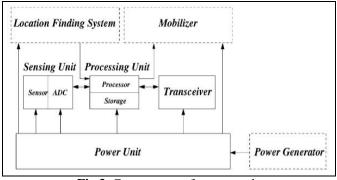


Fig 3. Components of sensor node

The wireless sensor nodes are micro-electric devices with a limited power source $\{0.5V, 12V\}$. Depending on the application, the need for power increases or decreases [2]. To meet the requirements of sensor networks, the sensor nodes show a strong dependency on battery life time. The main task of a sensor node in network is to detect an event, perform quick local data processing and transmit data. Thus to perform these tasks, the power consumption is divided into three domains which are sensing, communication and data processing.

The sensing unit basically comprises of some special function devices like ADC or DAC's. The sensing power varies with the nature of application. Sporadic sensing might consume lesser power than constant event monitoring. The complexity of event detection also plays an important role in determining energy expenditure.

The sensor nodes and hardware associated with it consumes maximum energy in data communication. Mixers, frequency synthesizers, voltage controlled oscillators and power amplifiers, all consume valuable energy and power in the trans-receiver circuitry. The active power as well as the start-up power consumption in the circuitry is considered. The power consumption for a radio (wireless network) is given by (3).

:
$$P_{C} = N_{T}[P_{T}(T_{ON} + T_{st}) + P_{out}(T_{on})] + N_{R}[P_{R}(R_{on} + R_{st})]$$
 (3)

Where P_T and P_R is the power consumed by the transmitter and receiver respectively, P_{out} is the output power of the transmitter, T_{ON} and R_{ON} is the on time of transmitter and receiver, T_{st} and R_{st} are the start up time of transmitter and receiver and N_T and R_T are the number of times transmitter and receiver is switched ON per unit time. In order to achieve low power consumption, rearrangements and conversions are to be done in the architecture and designing of sensor networks.

The power consumption in data processing is given by : $P_P = CV_{dd}^2 f + V_{dd} I_0 e^{Vdd/nV} f$ (4). Here C is the total switching capacitance, V_{dd} the voltage swing and f is the frequency.

III. Processor's choice in a sensor network

Microprocessors and Microcontrollers are used as a processor for various wireless sensor networks. The features [3] to be considered or the architecture of processor includes:

III.1 Wake up time: A widely used goal for sensor applications is an average duty cycle of 1%. This is achieved by scheduling events for some time in the future and then sleeping. Most microcontrollers implement an asynchronous timer which is clocked, while the core and other peripherals are powered off. An interrupt is triggered when the timer rolls over to wake the system from sleep. Interfacing with external hardware often results in waiting times in the core. A typical sequence consists of setting some bits, waiting a number of milliseconds, changing the settings, waiting some more milliseconds and so on. If the wake up is sufficiently fast, the core may sleep while waiting.

III.2 Clock Scaling: Some microcontrollers can dynamically switch their operating frequency, either by using a divider on the primary system oscillator or a low-frequency oscillator with a controllable multiplier. The first approach runs the oscillator at full speed, dissipating maximum power, but the system logic operates at a lower speed and lower power. The multiplier has its own power overhead, and may require time to settle if the multiplying factor is changed. The multiplier based approach saves power by running a low- speed oscillator. There is usually a 32 kHz oscillator for timing purposes, such that there is no power overhead apart from that of the multiplier itself.

III.3 Input/Output Issues: Since the microcontroller is required to control a number of other devices, it must have a large number of digital I/O pins available for general use. Digital sensors will generally have a serial interface, but this may still require up to four or five pins per sensor, as will an external FLASH memory. Equally important is the logic behind them. Serial interface logic can allow the shifting out of digital data to be carried out in the background, while the microcontroller core is powered down. Almost all microcontrollers contain a hardware UART, which can be used to control a standard serial port, using an external level-shifting chip.

III.4 Memory Architecture: When servicing an interrupt, the handler will often have to save a number of registers and flags before executing anything. Since an interrupt handler will generally execute very little code, this can also come to dominate the time for which the core is active. The most efficient solution would be to have two completely separate sets of registers, and switch between them using a banked access, allowing the context switch to take place in a single instruction. The advantage of a dynamic stack is that any configuration of functions can be supported, and functions can be reentrant. The disadvantage is that some embedded architectures may not have dedicated stack access instructions. In a compiled stack all memory accesses are static, because the address is determined at compile time, resulting in efficient memory access.

IV. Conclusion

While the microcontroller is a central part of any wireless sensor node design, little consideration has gone into choice of device in the past. There are a wide range of microcontrollers currently in the market which offer broadly similar features. Node lifetime is determined by battery life, so power conservation is the prime concern. The type of memory and memory access instructions determine how efficiently the code will execute. An overhead of a few instructions per memory access can significantly influence the executing duty cycle and power dissipation. More complex instruction sets can also speed up processing tasks, allowing the system to spend more time sleeping. A useful feature is the ability to self-program. In order to generate efficient code, a well-optimized version of gcc or a similar flexible, optimizing compiler for the target architecture is a major advantage. However, due to the design of gcc, it does not deal well with accumulator-based architectures such as the PIC. Sensor nodes and wireless sensor networks have a wide ranging applications in military field, environmental issues, home appliances, health issues and other commercial purposes like managing inventory, building virtual keyboard, managing product quality, constructing smart office spaces, robot control etc.

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