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Analysis and Implementation of PID Controller Design

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Abstract
This report presents the Implementation of PID controller on FPGA using Xilinx ISE 14.7. Main concerns of these project are to tune parameters using MATLAB. This paper presents the RTL design, synthesis, and implementation of VHDL code is carried out using Project Navigator ISE 14.7 software. The simulation is visualized using ISIM simulator. Xilinx device of Spartan Family Spartan 6 is used for hardware evaluation. The system used is second order state system.

Keywords: *PID Controller, Proportional, Integral, Differentiator, RTL Design, Result analysis, VHDL Programming, MATLAB Programming.*

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I. Introduction

Idea of Implementation

PID stands for Proportional Integral Derivative controller. It is used for closed loop industrial automation process control specially to control process variables as temperature, pressure. The three controllers combinedly adjust output levels as part of feedback signal. The first PID controller was developed by Elmer Sperry in 1911 around 100 years back. FPGA implementation is used for complex functionality, low power consumption, real time processing ability, high speed computation. This system does not require precise analytical model of control process to be implemented. Today PID controllers are rapidly used in areas as process control, robotics, transportation systems, automation, manufacturing, and aerospace.

PID controller Implementation can be done by various methods-

1. Analog electronic component combination
2. Software programming implementation
3. Implementation using FPGA

Steps of Implementation can be various methods-

1. Mathematical Modeling
2. Designing of Controller

Types

1. Proportional Type controller-

It is manually turned ON and at threshold value, Output is turned OFF and helps in power reduction.

2. ON/OFF Type PID Controller-

At threshold value, Output is turned ON and manually Turned OFF once its functionality is achieved.

3. Real Time Standard controller-

It defines function within itself and works as PI or PD or ID controller as well for requirement. Combination of two PID controllers can be present as well with solo and twin cascade control loop.

II. Literature Survey

Block Diagram

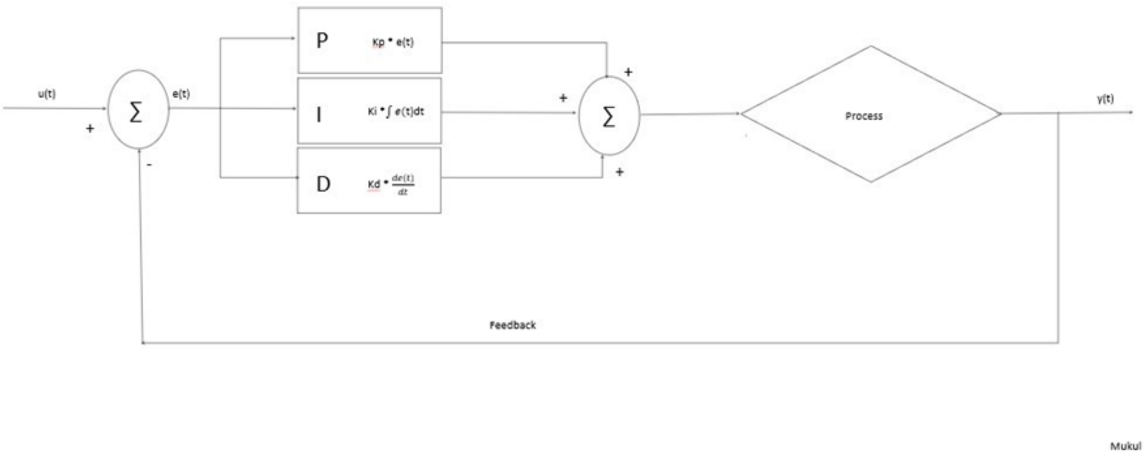

Diagram 1- PID Controller Architecture

Working

PID Controller is feedback system. Signal from PID block controls Process. Part of Output signal is compared with input signal and error signal is generated. Error signal can be Zero or fixed value depend on process driven by it. The proportional gain, derivative gain and integral gain are represented by Kp, Kd and Ki respectively. Because of Proportional constant Kp , control signal reacts to error immediately, but error does not nullify . Hence, Integral constant Ki helps to lessen effect of offset error. Oscillations are dampened due to Derivative constant Kd .

Controller can be Either ON or OFF.

$$y(t) = Kp * e(t) + Ki * \int e(t)dt + Kd * \frac{de(t)}{dt}$$

$$Output = [Kp + Ki/s + Kd*s]* Error$$

Tunning

Once PID controller is installed in System, we need to tune it with variables to controlled it with proper values of P, I and D. Although designers provide values, it can’t always work for those values and affects system stability and performance.

Tunning of PID controller can be done by various methods-

1. Process Reaction Curve

Open loop step response is recorded for some output arbitrarily decided. Then from parameters of output, gain factors are calculated.

2. By Trail Error

First set Ki=0, Kd=0 and adjust Kp to oscillating output. Then adjust Ki for stable output and Kd for faster response.

III. Specifications

PID controller Specifications taken Under Consideration.

□	Input Data Pins	:	16
□	Input Control Pins	:	2 (Clock)
□	Output Data Pins	:	16
□	ADC Pins	:	16

□	DAC Pins	:	16
□	Reset	:	1
□	Operating Clock	:	33 MHz
□	P	–	20
□	I	–	10
□	D	–	1
□	PI	–	6.78
□	PD	–	0.9523
□	ID	–	1.1
□	PID	–	5.297

Top Level Diagram

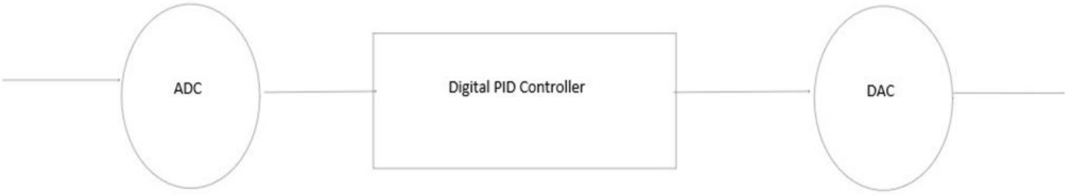

Diagram 2- PID Controller µ-Architecture

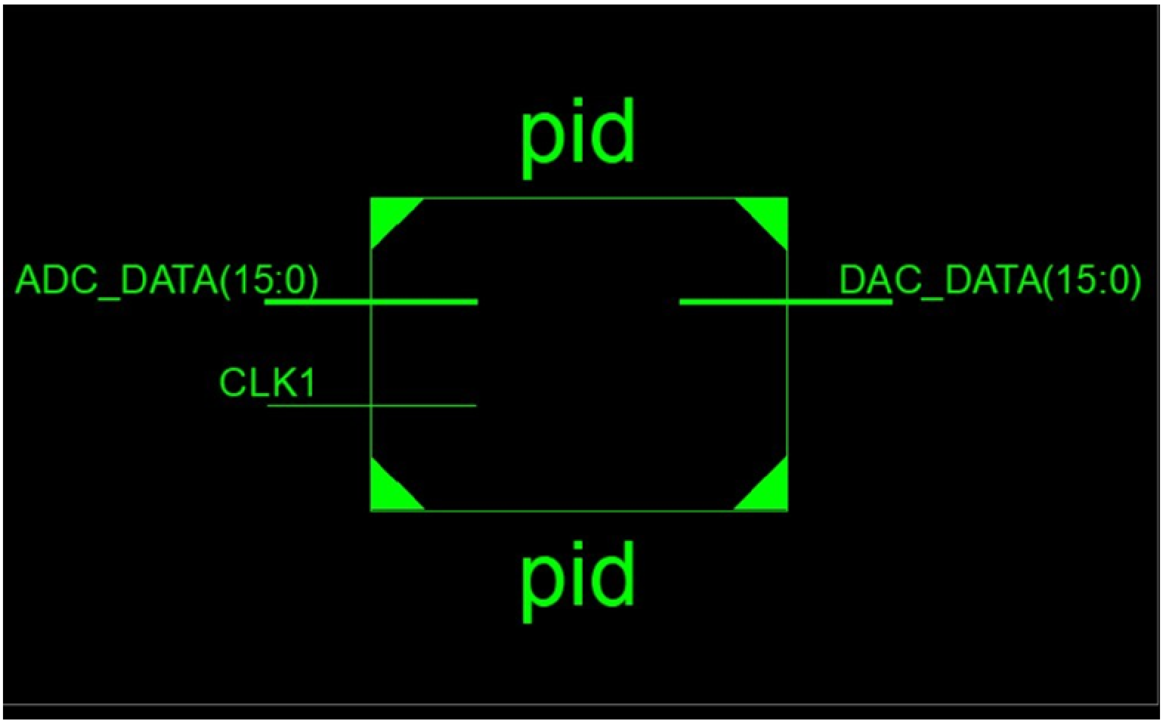

Diagram 3- PID Controller Top Level Diagram

IV. Prerequisites

FPGA (Field Programmable Gate Array)

FPGAs are semiconductor devices consisting of a matrix with Configurable Logic Blocks connected with programmable interconnects. FPGAs are reprogrammed for desired functionality based on requirements after manufacturing. It distinguishes FPGAs from ASICs which is customized for special tasks. Now multiple advanced FPGAs are available with a greater number of functionalities. These chips have on board DSP processor, memory (Block RAM), Digital Clock Manager (DCM), Input Output Block (IOBs), Configurable Logic Blocks (CLBs). Fig1.3 shows functional blocks of FPGA.

Xilinx ISE Design Suite - Webpack Edition

Xilinx ISE Design Suite is a software designed by Xilinx Inc. for synthesis and analysis of hardware designed using HDLs. It enables users to synthesize designs, perform timing analysis, view RTL diagrams, and configure target device. ISE Webpack provides design flow providing access to the ISE functionality free of cost.

SPARTAN 3E FPGA Board

The board provides a platform for design to implemented on Xilinx Spartan 3E FPGA.
This board features 500,000 gates for a complex and high-volume designs and 64 MB DDR RAM. It supports USB and JTAG parallel programming interface. It has LCD and LED interfaces for testing purpose.
6.Proportional Control

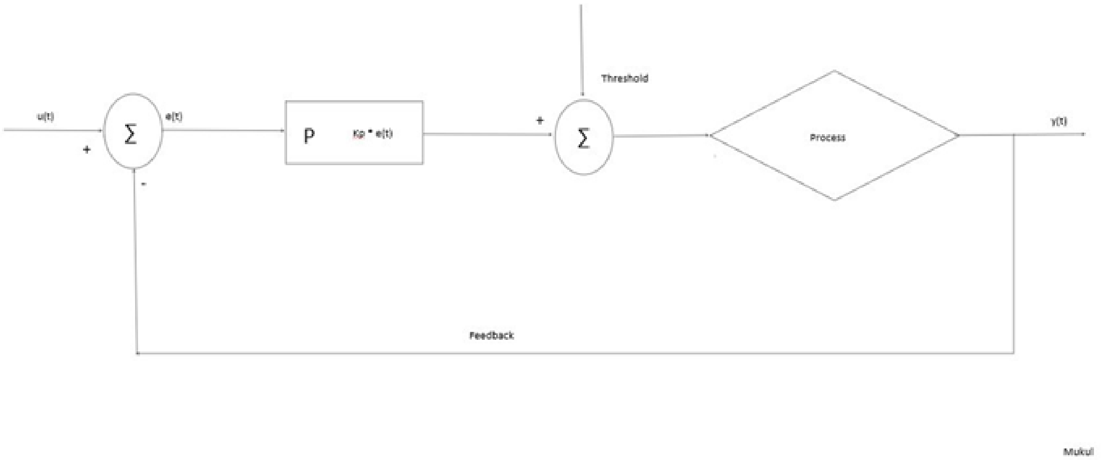

Diagram 4- P Controller Diagram

Working

Output signal is proportional to error signal. Biasing or manual reset is needed for controlling output as it does not achieve steady state.

$$y(t) = Kp * e(t)$$

$$\text{Output} = [Kp]* \text{Error}$$

V. Integral Control

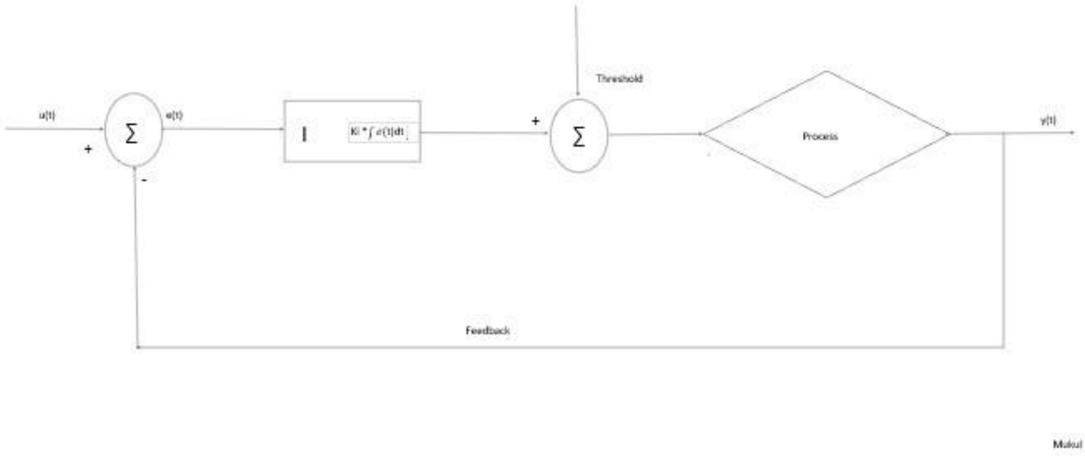

Diagram 5- I Controller Diagram

Working
Output signal is integral of error signal. It helps in removing steady state error. But for negative error output decreases and stability of system is affected.

$$y(t) = Ki * \int e(t)\, dt$$

Output = [Ki / s] * Error

8.Derivative Control

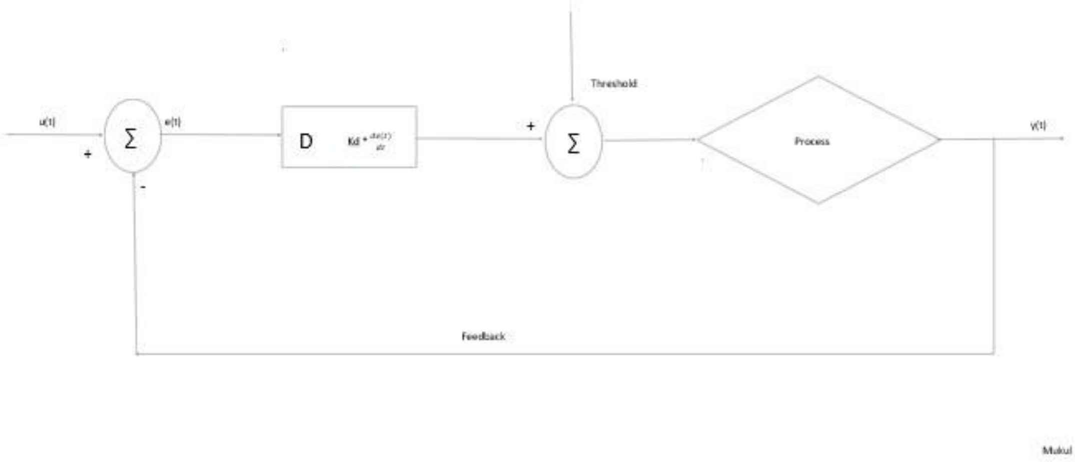

Diagram 6- D Controller Diagram

Working
Output is signal is rate of change of error signal related to time. It helps in predicting upcoming error signal behavior and settling time reduces.

$$y(t) = Kd * \frac{de(t)}{dt}$$

Output = [Kd * s] * Error

Additional Blocks

Feedback Block

Feedback Block is used to feed part of Output signal to input and represented by wire.

Summing Block

Summing Block is used to sum or find difference between Input signal and Feedback Signal depending on decision by Comparator Block.

Comparator Block

Comparator Block is used to find comparison between Input signal and Feedback Signal depending on Threshold decided by User.

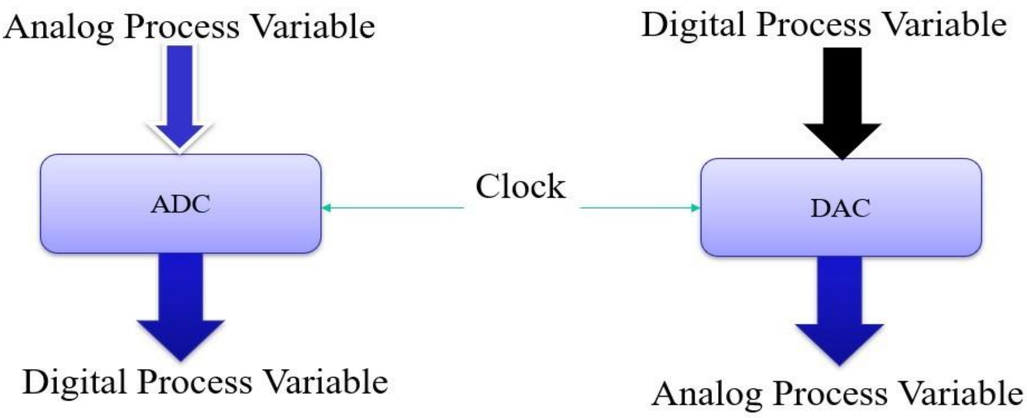

Diagram 7- ADC DAC Controller Diagram

ADC Block

ADC Block is used to convert Analog Input to Digital Output and can be used for Input Signal or Feedback Signal depending according to User System requirements.

DAC Block

DAC Block is used to convert Digital Input to Analog Output and can be used for Input Signal or Feedback Signal depending according to User System requirements.

10.Synthesis Report

HDL Synthesis

FSMs	:	1
Multipliers	:	2 32x32 bit
multiplier	:	2
Adders/Subtractors	:	8 32-bit
adder	:	3
32-bit subtractor	:	2 33-bit
adder	:	3
Latches	:	11
16-bit latch	:	3
32-bit latch	:	8
Comparators	:	4
32-bit comparator great/equal	:	1
32-bit comparator greater	:	1
32-bit comparator less	:	1
32-bit comparator less/equal	:	1

Registers	:	7
Flip-Flops	:	7
Shift Registers	:	18 2-bit
shift register	:	18

```
Design_Statistics
IOs                          :          33

Cell Usage
BELS                         :         756
GND                          :           1
INV                          :          65
LUT1                         :          40
LUT2                         :         128
LUT3                         :          12
LUT4                         :          49
MUXCY                        :         238
MUXF5                        :           1
VCC                          :           1
XORCY                        :         221
FlipFlops /Latches           :         219
FD                                  :          25 LD                          :          194

Shift Registers          :          18
SRL16                           :          18

Clock Buffers            :           5
BUFG                     :           4
BUFGP                    :           1

IO Buffers               :          32
IBUF                     :          16
OBUF                     :          16

MULTs                    :           4
MULT18X18SIO             :           4


Device utilization summary:

Selected Device : 3s500evq100-5

Number of Slices                        :          226  out of   4656     4%
Number of Slice Flip Flops                        :          187  out of   9312     2%   Number of 4 input
LUTs                     :          312  out of   9312     3%
Number used as logic                              :          294
Number used as Shift registers                    :          18
Number of IOs                                     :          33
Number of bonded IOBs                               :          33  out of     66    50%
IOB Flip Flops                                    :          32
Number of MULT18X18SIOs                 :          4  out of     20    20%   Number of GCLKs
                         :          5  out of     24    20%


Timing Summary

Minimum period                                       : 4.795ns (Maximum Frequency: 208.542MHz)
Minimum input arrival time before clock           : 1.731ns
Maximum output required time after clock : 4.114ns Maximum combinational path delay              : 6.317ns

Timing constraint
Clock period                                         : 1.855ns (frequency: 539.041MHz)
```

11.Real Time Literature Survey

Advantages

- Better rise time and settling time
- Reduce error and cost of the system design
- Minimizes the Power Consumption and Delay
- Combinedly used according need

Disadvantages

- Longer processing cycles
- Auto calculation and tuning of parameters required
- Hardware architectural design affect performance
- Latent width controllers

Applications

- In Power Electronics Converters to activate IGBTs
- In Automatic Temperature Controlled HVAC Systems.
- In Photovoltaic cell to control MPPT Charge

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Future Scope

PID Controller can be directly used as Global IP on FPGA as it is most used component and will be directly available for use. Power Optimization can be worked on as well.

VI. Conclusion

Contribution

- Implementing PID controller on FPGA using HDL
- Speed, Accuracy & Power over other implementation techniques.
- PID Constants Tunned using MATLAB.
- FPGA utilization compression and optimization achieved.
- Digitally faster performance was achieved.

Conclusion

For Step response of system, Increment in Kp will lead to reduction in the steady state error and rise time, but after specific limit it will only increase overshoot. Increment in Ki removes steady state error and rise time, but after specific limit it will only increase overshoot. Increment in Kd reduces the overshoot and settling time.Use of Multipliers help in reducing settling and rise time.

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Finally, I would like to express thanks from bottom our heart to everyone who directly or indirectly help me during this project.

I am going to use property of impedance which changes accordingly material deformation or combination for different application.