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Plasma Processing Of A Semiconductor Surface For Cleaning And Growing An Oxide For MOS Devices

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Abstract: *This article researches and reviews plasma processing on Si surfaces for cleaning the Si surface by removing the native oxide and also growing a low temperature oxide on the cleaned surface. The 6.3nm low temperature oxide is also separately characterized for thin film transistor application. The author performed research in this area during his doctoral research work and research work as a Scientist-'B' at the Institute of Technology, Banaras Hindu University (now IIT since 2012) from the period of 1989 to 1996 after which he went to USA for post-doctoral research work from 1996 to 2001.*

Keywords: *Plasma Processing, MOS device, Silicon, Silicon Carbide, Semiconductor.*

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I. Introduction

Plasma processing on the Si surface is mainly used for cleaning the organic carbon contaminants by about a 30s oxygen plasma treatment as a cleaning process. The author has investigated plasma processing for cleaning the Si surface by removing the native oxide in a CF_4/H_2 plasma and in-situ growing a thin 2-4 nm RF oxygen plasma oxide before thermal oxidation. Also, a 6.3 nm oxygen plasma oxide is grown in a barrel reactor at 1.0 Torr dynamic pressure and characterized for the application as a low temperature oxide. These investigations are now reviewed after getting the reactions from the other research groups around the world. Plasma processing is now also attempted on Silicon Carbide semiconducor surfaces.

II. Theory

Floating a Si sample in a RF oxygen plasma can cause a negative self-bias built on the sample that encourages positive ion bombardment of the Si surface. Atomic oxygen species can diffuse on to the sample surface and can cause cleaning of the carbon contaminants and also grow a thin plasma oxide if the time is elongated. A good study reference is a book by Chapman [1], which the author used as a text book for a graduate course study on Plasma Processing at University of Cincinnati, USA during 1988-89, though the plasma Processing field is vast with microelectronic applications of cleaning, etching and deposition. Many books and research studies are documented in this field.

III. Results and Discussion

The theoretical and experimental research on Si-based MOS devices was undertaken by the author as part of the Ph.D. research study in the period 1989 to 1996 along with a Ph.D. student who joined in 1994. The theoretical study was limited to finding the theoretical capacitance-voltage curve for a MOS device to implement the Terman technique of finding the interface trap density in a Metal-Insulator-Semiconductor (MIS) device with the thermal SiO_2 as an insulator abbreviating the device as a MOS device [2-5]. The electrical breakdown strength in the thermal oxide on one of the plasma cleaned Silicon surface was low at about 1 MV/cm. The low electric field is attributed to fringing fields on the sample holder and not the quality of the thermal oxide [5]. The relative increase in the electric field strength is still demonstrated on the sample where it is shown that the field strength increased to 1.63 MV/cm after plasma cleaning [5].

The concentration of the experimental research was on finding application of plasma processing that could be innovative and useful. Plasma cleaning of the Si surface was attempted in a CF_4/H_2 plasma (a form of etching) followed by in-situ oxygen plasma to grow an ultra-thin plasma oxide of about 2-4 nm on the cleaned surface. Dry thermal oxide grown at 1100^oC in 75% O_2-N_2 oxidation ambient on this cleaned surface showed reduced fixed oxide charge density thought to be due to prevention of regrowth of the native oxide after plasma cleaning and changing the oxidation kinetics favourably [6-8]. Forming gas annealing in 25%H_2-N_2 mixture at 400^oC for 8 minutes showed passivation of the fixed oxide charges in a thermal oxide grown on plasma cleaned Si surface without the plasma oxide. The fixed oxide charge density reduced from low $10^{11}/cm^2$ to low $10^{10}/cm^2$ due to the above forming gas annealing [9]. The passivation of the fixed oxide charges is an indication that they

are not "fixed" in the true sense of the word. It has been shown by Razaouk and Deal in 1979 that, low temperatureH_2 anneal can reduce the interface state density but not affect the fixed oxide charge density [10]. The true fixed oxide charge density is only in the low $10^{10}/cm^2$ after forming gas annealing. This means that the reduced fixed oxide charge density of 5-9 x $10^{10}/cm^2$ from 3.75 x $10^{11}/cm^2$ in MOS device [6-7], having thermal oxide grown on plasma cleaned Si surface with the plasma oxide can also be passivated by the forming gas annealing so as to lose the advantage of plasma cleaning with the plasma oxide grown over the cleaned Si-surface. Technically, the fixed oxide charge density of the thermal oxide grown over the plasma cleaned Si surface with a plasma oxide did reduce to $10^{11}/cm^2$ level or lower [6-7], which was lower than the charges in the oxide grown over the conventionally cleaned Si surface or the plasma cleaned Si surface without the plasma oxide [5-9]. But the forming gas annealing would further reduce the fixed charges to low $10^{10}/cm^2$ losing the advantage of plasma cleaning with or without the plasma oxide. An unclean control sample showed fixed oxide charge density in the 2 x $10^{12}/cm^2$ order clearly indicating the need for cleaning the Si surface before oxidation [11]. A 6.3 nm near-room temperature plasma oxide was characterized for the properties of interface trap density and fixed oxide charge density in the oxide. The oxide showed high densities of the order of 5 x $10^{12}/cm^2$ with 40-60 mV of hysteresis in the capacitance-voltage plot indicative of high interface trap density [11]. The current-voltage characterization also showed that the oxide is leaky and technologically not useful as a gate oxide [11]. Plasma enhanced chemical vapor deposited (PECVD) oxide using pure SiH_4 (Silane) and N_2O gases was also researched on. The MOS devices with the deposited oxide were characterized resulting in a good idea that a long time of 40 min annealing in N_2 ambient post metallization, can cause densification of the deposited oxide and reduction in the leakage current [12]. More than 40 min annealing degrades the interface [13]. The substrate temperature for the deposition was found to be 250^{o}C to 350^{o}C as the suitable range and a pre-deposition cleaning in H_2 plasma can eliminate hysteresis and bias-instability in the capacitance-voltage plot [12-13].

Although, plasma cleaning of the Si surface was tried and was found technically effective, another two research studies later on showed that dilute HF cleaning could be more effective in reducing the interface trap level densities and the atomic O and F concentrations on the Si surface after cleaning [14, 15]. In particular, Metzler et al. [15] showed in Fig 9 (c) and (d) of his research that the O1s and F 1s intensities after native oxide removal, were much lower on the Si surface after dilute HF etching as compared to plasma etching. Chang et al. [14] also showed that the Si cleaning process C4B having a 1:200 dilute HF as the last etch gave the lowest interface trap density as shown in Fig 3 of their study with a high oxide breakdown field of 10-11 MV/cm [14]. Keep in mind that the oxide/silicon interface of the MOS device was hydrogen passivated. Hydrogen passivation actually hides the effect of cleaning by passivating the reduced oxide densities after cleaning also. A positron study of plasma-treated silicon wafers show reduced interface trap and fixed oxide densities in H_2 plasma treated Si surface although UV damage occurs [16], promoting the idea of the use of remote plasma.

Low-temperature oxide is the need for thin-film transistors in active matrix liquid-crystal displays and the room temperature RF oxygen plasma oxide grown at 1.0 Torr dynamic pressure was investigated by the author and is discussed above as one such attempt. The oxide showed 5-7 MV/cm oxide breakdown and high interface trap level density of about 7 x $10^{11}/cm^2eV$ in the MOS device on Si surface [11]. Another study by Fan et al. [17] that an oxygen plasma oxide on the SiGe substrate grown at 0.1 Torr pressure and less than 100^{o}C ambient temperature was stoichiometric and had low leakage current in the NMOS device making it a suitable low temperature oxide.

IV. Conclusions

Plasma cleaning of the Si surface technically is effective in reducing the fixed oxide charges in the MOS device having a thermal oxide grown after plasma cleaning but the low temperature forming gas annealing usually performed on Si MOS devices will hide the effect of cleaning by reducing them further to low $10^{10}/cm^2$ order. Also, the O1s and F1s intensities on dilute HF cleaned Si surface are significantly lower than in plasma cleaned Si surface. The low temperature plasma oxide grown in oxygen plasma is stoichiometric and can be considered for thin film transistor application.

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