Design of an Optimized Modulation for AC-DC Harmonic Immunity in VSC HVDC Transmission

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Abstract: *Control methods based on selective harmonic elimination pulse-width modulation (SHE-PWM) techniques offer the lowest possible number of switching transitions. This feature also results in the lowest possible level of converter switching losses. For this reason, they are very attractive techniques for the voltage-source-converter-(VSC) based high-voltage dc (HVDC) power transmission systems. The paper discusses optimized modulation patterns which offer controlled harmonic immunity between the ac and dc side. The application focuses on the conventional two-level converter when its dc-link voltage contains a mix of low-frequency harmonic components. Simulation and experimental results are presented to confirm the validity of the proposed switching patterns.*

Key words: *Amplitude modulation (AM), dc-ac power conversion, harmonic control, HVDC, insulated-gate bipolar transistor(IGBT), Power electronics, power transmission system, pulse-width modulation, voltage-source converter (VSC).*

I.   Introduction

THE CONTINUOUS growth of electricity demand and ever increasing society awareness of climate change issues directly affect the development of the electricity grid infrastructure. The utility industry faces continuous pressure to transform the way the electricity grid is managed and operated. On one hand, the diversity of supply aims to increase the energy mix and accommodate more and various sustainable energy sources. On the other hand, there is a clear need to improve the efficiency, reliability, energy security, and quality of supply. With the breadth of benefits that the smart grid can deliver, the improvements in technology capabilities, and the reduction in technology cost, investing in smart grid technologies has become a serious focus for utilities. Advanced technologies, such as flexible alternating current transmission system (FACTS) and voltage-source converter (VSC)-based high-voltage dc (HVDC) power transmission systems, are essential for the restructuring of the power systems into more automated, electronically controlled smart grids.

An overview of the recent advances of HVDC based on VSC technologies is offered. The most important control and modeling methods of VSC-based HVDC systems and the list of existing installations are also available.

The first generation of utility power converters is based on current-source converter (CSC) topologies. Today, many projects still use CSCs due to their ultra-high power capabilities. With the invention of fully controlled power semiconductors, such as insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors (IGCTs), the VSC topologies are more attractive due to their four-quadrant power-flow characteristics. A typical configuration of the VSC-based HVDC power transmission system is shown in Fig. 1 as it is shown.
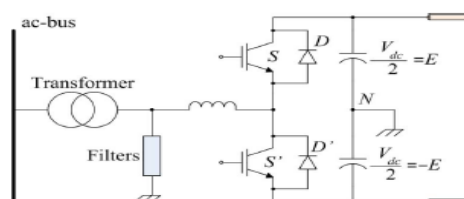

Fig. 1. Phase of the two-level VSC for the HVDC power transmission system

The multilevel topologies for high-voltage high-power VSCs are also briefly discussed. Multilevel converters can be more efficient but they are less reliable due to the higher number of components and the complexity of their control and construction. Increasing the number of levels above three is a difficult task for

the industry. The multilevel converters are beyond the scope of this paper. This paper focuses on the conventional three-phase two-level VSC topology (Fig. 2) and associated optimized modulation.
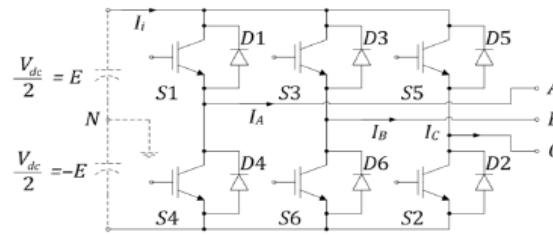

Fig. 2. Three-phase two-level VSC.

In most cases, the voltage of the dc side of the converter is assumed to be constant and the ac network is assumed to be balanced. However, fluctuations at various frequencies often occur on the dc side which usually appears as harmonics of the ac-side operating frequency. The most significant harmonic introduced to the dc-side voltage spectrum by an unbalanced three-phase ac-network is the 2nd harmonic. Inverters with 2nd harmonic on the dc bus generate the third harmonic on the ac side the elimination of inverter low-order harmonics with fluctuating input voltage is described.

The proposed M-type modulation technique allows 33% reduction in the switching transitions without lowering the order of the predominant harmonic. The geometrical technique of proposes a numerical calculation by modifying the Pulse width to cancel the harmonics produced by the dc-side ripple voltage. It has lower total harmonic distortion (THD) when compared with the conventional triangular sinusoidal PWM in the case where the dc-link voltage also fluctuates. However sinusoidal-PWM techniques, which require a relatively high number of transitions per cycle to eliminate the low-order harmonics. Selective harmonic elimination pulse-width modulation (SHE-PWM) is the harmonic control with the lowest possible switching to give tightly controlled voltage spectrum and increase the bandwidth between the fundamental frequency and the first significant harmonic.

In the last decade or so, the size and level of power handling capability of the VSCs has increased substantially and has reached new heights for utility applications. As the interaction between the dc and ac systems increases and the power handling capability of these converters increases, it is important to further understand and study the effects of voltage and current harmonics on the converter design and operation and system performance. Any measures to minimize or even eliminate such unnecessary flowing of harmonics between the two systems (i.e., the ac and dc) are beneficial.

For instance, an approach that determines the harmonic spectrum of the dc-bus currents of VSC sis presented. For a two-level three-phase VSC, a general method for calculating the dc-bus currents for unbalanced, balanced, linear, and nonlinear loads is described. Ways to select the appropriate dc-link capacitor for VSCs and voltage-stiff-inverters are analyzed respectively. A method to reduce the dc-bus capacitor ripple current of an induction motor with constant volt/Hertz is investigated. However, even if the converters have less dc-side ripple voltage with smaller dc-link capacitors than conventional methods, the capacitors remain one of the components most prone to failure. Minimizing or eliminating harmonic flows in the dc-link capacitors will decrease the dissipated heat and increase overall reliability and efficiency. On the other hand, optimized modulation methods offer many advantages toward tight control of converter-generated harmonics. A minimization method to find the complete set of solutions by solving the SHE-PWM equations for two-level inverters is discussed. In this paper, the dc-link voltage is assumed to be constant.

A method is proposed to prevent the dc-link ripple voltage from creating low-order harmonics on the ac side of fixed and variable frequency inverters. However, only one of the multiple SHE-PWM set of solutions is reported. An investigation of the harmonic interaction between the ac and dc side for STATCOM is presented including the so-called dynamic SHE-PWM scheme based on precalculated angles for better THD. However, the dynamic SHE-PWM scheme is applied only for a three-level converter and can be applied only for known magnitude and frequency of the ripple. Another method for improving the harmonic performance of a two-level VSC with SHE-PWM is studied. However, only one set of SHE-PWM solutions is considered for the method of which requires the exact values of magnitude, phase, and frequency of the ripple in order to be implemented.

Control strategies to compensate unbalances are reported in the literature. Mild imbalances caused by unbalanced loads of the ac side are regulated by using separate control loops for the positive- and negative-sequence components of the voltage as proposed. Efficient control of unbalanced compensator currents can be achieved by a control algorithm based on the D-STATCOM model. D-STATCOM allows separate control of positive- and negative-sequence currents and decoupled current control of the − frame.

An advanced strategy based on direct power control under unbalanced grid voltage conditions has been recently presented for a doubly fed induction generator. To take the full advantages of VSCs for HVDC power transmission systems, an auxiliary controller is added to the main controller which is conventionally

implemented in the positive-sequence – frame. To compensate for unbalanced ac-side loads, the auxiliary controller is implemented in the negative-sequence – frame. The objective of this paper is to discuss the effectiveness of optimized modulation based on precalculated SHE-PWM in a two-level three-phase VSC to make the ac side immune from the fluctuations of the dc link without the use of passive components. However, since the VSC studied here does not include a closed-loop controller, strategies to compensate unbalances are not addressed in this paper. This paper is organized in the following way. In Section II, a brief analysis of the VSC and the modulation method is provided. Section III contains the characteristics of the method on a VSC with dc-side ripple voltage. Section IV provides extensive experimental results to support the theoretical arguments. Conclusions are documented in Section V.

II. ANALYSIS OF THE PWM CONVERTER AND SHE-PWM

The optimized SHE-PWM technique is investigated on a two level three-phase VSC topology with IGBT technology, shown in Fig. 2. A typical periodic two-level SHE-PWM waveform is shown in Fig. 3.The waveforms of the line-to-neutral voltages can be expressed as follows:

$$V_{LN} = \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = V_{dc} \begin{bmatrix} \sum\limits_{n=1}^{\infty} A_n \sin n\omega_o t \\ \sum\limits_{n=1}^{\infty} A_n \sin n\left(\omega_o t - \frac{2\pi}{3}\right) \\ \sum\limits_{n=1}^{\infty} A_n \sin n\left(\omega_o t + \frac{2\pi}{3}\right) \end{bmatrix} \quad \text{……………….. (1)}$$

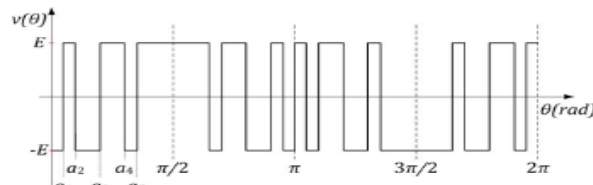When is the operating frequency of the ac, and is the dc-link voltage.

Fig.3. Typical two-level PWM switching waveform with five angles per quarter cycle.
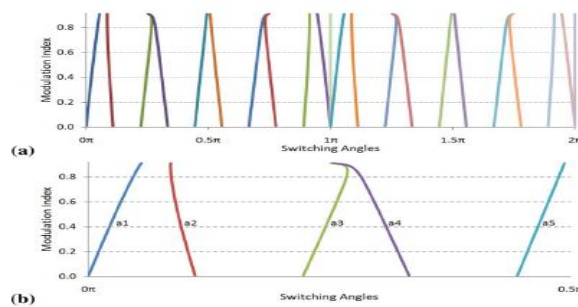

Fig. 4. Solution trajectories. (a) Per-unit modulation index over a complete periodic cycle.
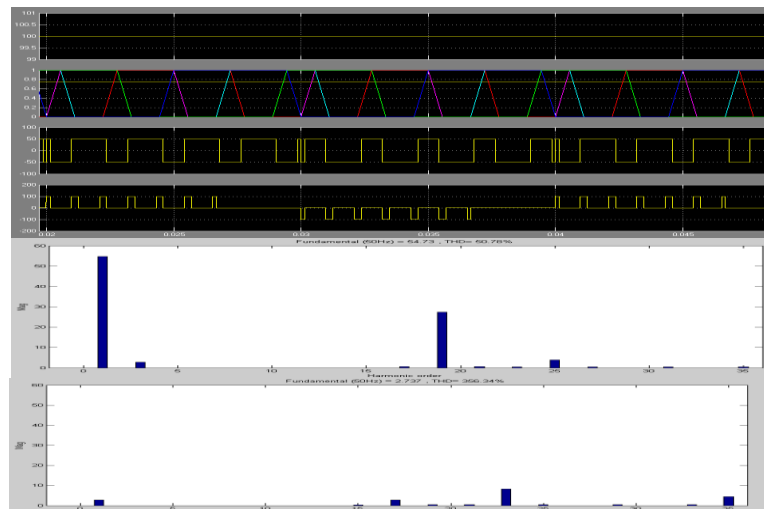(b) Five angles in radians.

Fig. 5. Simulation results for SHE-PWM eliminating 5th, 7th, 11th, and 13th harmonics. (a) DC-link voltage. (b) Solution trajectories to eliminate harmonics and intersection points with the modulating signal (M = 0.75).(c) Line-to-neutral voltage. (d) Line-to-line voltage. (e) and (f) Positive- and negative-sequence line-to-line voltage spectra, respectively

Thus, the line-to-line voltage are given by

$$V_{LL} = \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \sqrt{3} \cdot V_{dc} \begin{bmatrix} \sum_{n=1}^{\infty} A_n \sin n \left(\omega_o t + \frac{\pi}{6} \right) \\ \sum_{n=1}^{\infty} A_n \sin n \left(\omega_o t - \frac{\pi}{2} \right) \\ \sum_{n=1}^{\infty} A_n \sin n \left(\omega_o t + \frac{5\pi}{6} \right) \end{bmatrix} \quad \text{……………. (2)}$$

The SHE-PWM method offers numerical solutions which are calculated through the Fourier series expansion [20] of the waveform

$$M = 1 + 2 \sum_{i=1,2,3...}^{N+1} (-1)^i \cos(\alpha_i)$$

$$0 = 1 + 2 \sum_{i=1,2,3...}^{N+1} (-1)^i \cos(k\alpha_i) \quad \text{…………………. (3)}$$

Using five switching angle per quarter-wave (N = 4) in SHE-PWM, k=5, 7, 11, 13 to eliminate the 5th, 7th, 11th, and 13th harmonics. During the case of a balanced load, the third and all other harmonics that are multiples of three are cancelled, due to the 120 symmetry of the switching function of the three-phase converter. The even harmonics are cancelled due to the half-wave quarter-wave symmetry of the angles, being constrained by

III. Ripple Repositioning Technique:

In this section, the technique to reposition the low-order harmonics produced by the dc-link ripple voltage of a VSC is described. The switching angles are precalculated for every available modulation index to obtain the trajectories for the SHE-PWM, as shown in Fig. 4 .The complete sets of results are presented.

The intersections of the trajectories shown in Fig. 4 with any horizontal straight line, called the modulating signal (i.e., an imaginary line of M = 0.75p.u.), give the switching angles of the specific modulation index. Those switching angles are identical to the solution of the conventional SHE-PWM method, so when the dc bus voltage is constant, all harmonics before the 17th one are eliminated. However, when the dc bus voltage is fluctuating, other harmonics are introduced. When the dc link has a ripple voltage of constant frequency and amplitude times the dc-side voltage, the line-to-neutral voltage is represented as

$$V'_{LN} = V_{LN} \left(1 + k \sin \omega_r t \right) \quad \text{………………. (4)}$$
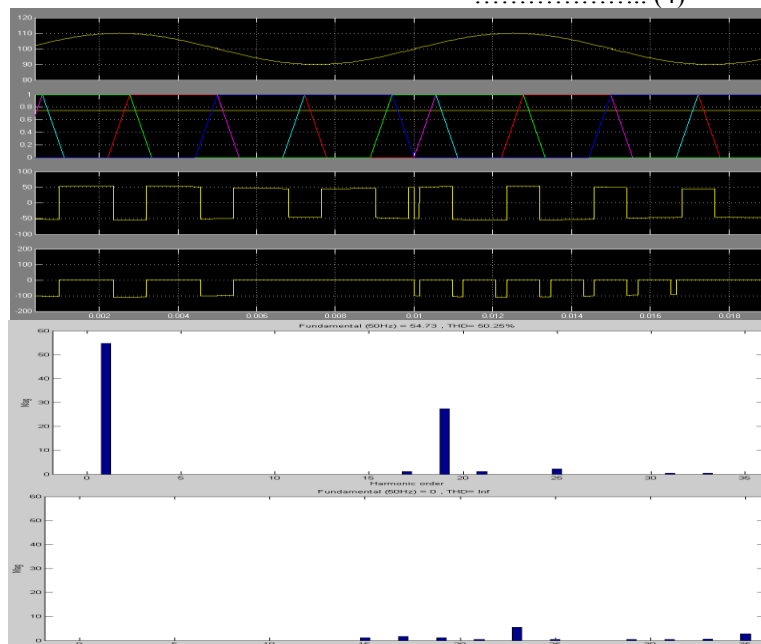
Fig. 6. Simulation results for conventional SHE-PWM with 10% ripple of 2nd harmonic at the dc bus (without the repositioning technique). (a) DC-link voltage with 10% ripple. (b) Solution trajectories to eliminate harmonics and intersection points with the modulating signal (M = 0.75) (c) Line-to-neutral voltage. (d) Line-to-line voltage. (e) and (f) Positive- and negative-sequence line-to-line voltage spectra, respectively

Therefore, the modified line-to-line voltage of (2) becomes

$$
\begin{aligned}
V'_{AB} &= V_{AB}\left(1 - k\sin\omega_r t\right) \\
&= \sqrt{3}\cdot V_{dc}\sum_{n=1}^{\infty}\left\{ A_n\sin n\left(\omega_o t + \frac{\pi}{6}\right)\right. \\
&\quad + \frac{k}{2}A_n\cos\left[(\omega_r - n\omega_o)t - n\frac{\pi}{6}\right] \\
&\quad \left. - \frac{k}{2}A_n\cos\left[(\omega_r + n\omega_o)t + n\frac{\pi}{6}\right]\right\}
\end{aligned}
$$
.... (5)

The method is used in the same way as in (5) to derive the other two line-to-line voltages of the three-phase converter and. As was already mentioned, unbalance on the ac network can cause the 2nd harmonic on the dc-side voltage. Hence, and by substituting in (5), the lower order harmonics are given by

$$
V_{h1} = \frac{\sqrt{3}}{2}V_{dc}A_1 k\cos\left(\omega_o t - \frac{\pi}{6}\right)
$$
.... (6)

$$
V_{h2} = \frac{\sqrt{3}}{2}V_{dc}A_1 k\cos\left(3\omega_o t + \frac{\pi}{6}\right)
$$
.... (7)

The negative-sequence fundamental component and the positive- sequence 3rd harmonic are created on the ac side since it is proven in (6) and (7), respectively. For a constant dc-bus voltage, the modulating signal is a straight line of magnitude equal to the modulation index.

For the fluctuating dc-bus voltage, the modulating signal is divided by $(1 + k\sin\omega_r t)$, which is the sum of the average per-unit value of the dc link and the ripple voltage in order to satisfy the repositioning technique. So when the magnitude of the dc-link voltage is instantaneously increased by a certain amount, the modulating signal's amplitude is reduced by using the switching angles of a lower modulation index.
Therefore, by using the higher modulation index at the instants that the voltage is reduced and lower modulation index at the instants that the voltage is increased, the amount of ripple is reversed. According to Fourier transform properties, multiplication in one domain corresponds to convolution in the other domain. So even if one frequency is removed from the modulated signal, it is expected to appear as sidebands of the switching frequency.
SW is the switching function of the conventional SHE-PWM and the new switching function is represented by
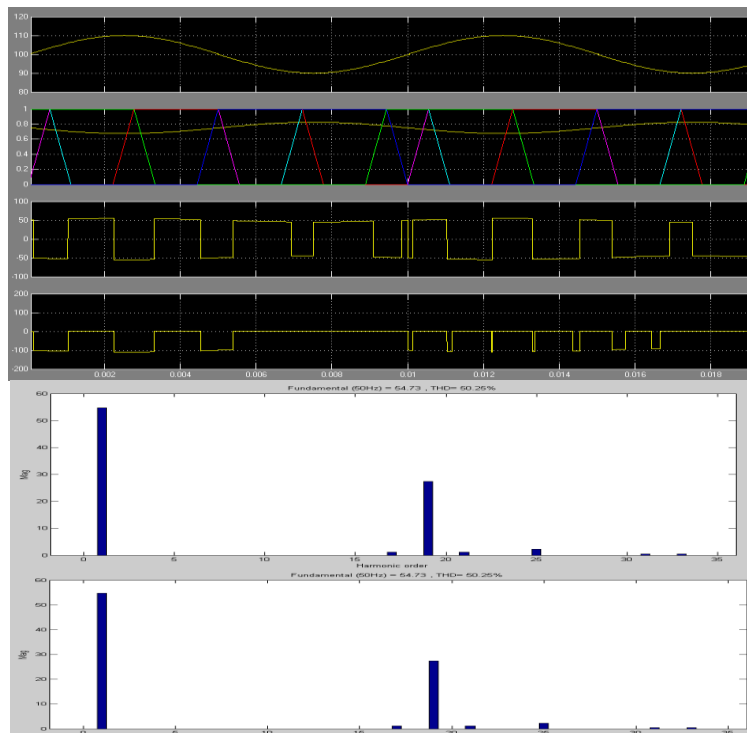
Fig. 7. Simulation results for 10% ripple of the 2nd harmonic at the dc bus by using the repositioning technique. (a) DC-link voltage with 10% ripple.(b) Modified modulating function and its intersection with the solution trajectories. (c) Line-to-neutral voltage. (d) Line-to-line voltage. (e) and (f) Positive- and negative-sequence line-to-line voltage spectra, respectively

$$SW' = \frac{1}{1 + k \sin \omega_r t} \cdot SW. \qquad (8)$$

Therefore, the relevant line-to-neutral voltage is given by

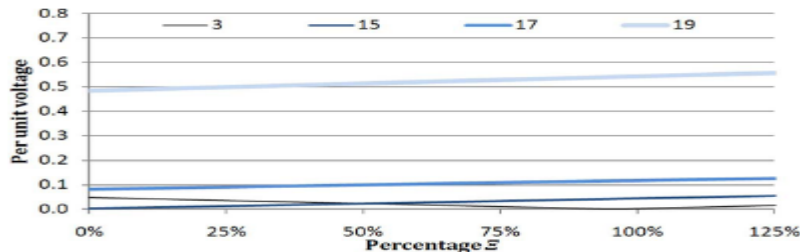$$V'_{LN} = V_{dc}(1 + k \sin \omega_r t) \cdot SW'. \qquad (9)$$

Fig. 8. Magnitudes of the significant harmonics with respect to the fundamental component while the percentage of ripple on increases.
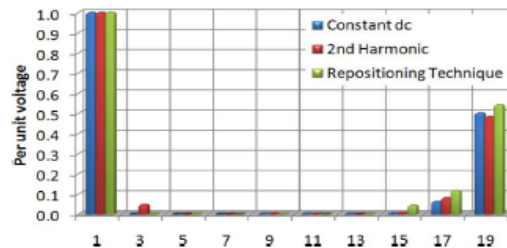

Fig. 9. Per-unit values of the low-order harmonics up to the 19th for the dc bus with a ripple of 10% 2nd harmonic.
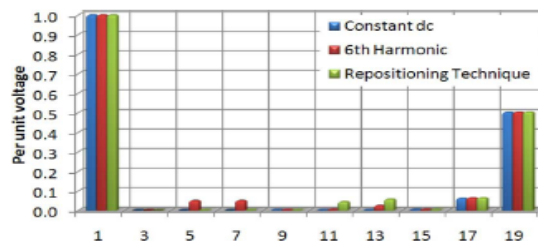

Fig. 10. Per-unit values of the low-order harmonics up to the 19th for a dc bus with a ripple of 10% 6th harmonic.

The new switching function has the property of nullifying the low-order harmonics of the ac side, produced by the ripple of the dc-side voltage. This new switching function is generated from the respective intersections of the modified modulating signal and the trajectories of harmonic elimination solutions.

A.   SIMULATION RESULTS:
The PSCAD/EMTDC software is used to demonstrate the dc-link ripple-voltage repositioning technique. Key results are presented in Figs. 5–7. Fig. 5 shows the simulation results of the method for the case that the dc-bus voltage has no ripple. The modulating signal is equal to the modulation index since the dc-link voltage is constant. Hence, the results are identical to the ones taken by using conventional SHE-PWM with a fixed modulation index
(m=0.75). Fig. 6 shows what happens when 10% of 2nd harmonic is added to the dc-link voltage. The switching angles are unchanged but the amplitude of the output voltage is fluctuating.
The modulating signal is forced to be constant to give the same results with the conventional SHE-PWM. The value of the fundamental component is increased by 5% and a value of the 3rd harmonic is equal to 5% of the fundamental that appears in the spectrum of Fig. 6(e).

By applying the dc-link ripple-voltage repositioning (Fig. 7), it is observed that the switching angles have slightly shifted. As shown in Fig. 7(e), the value of the fundamental component is equal to the one of Fig. 5(e).

The 3rd harmonic no longer exists. The modulating signal can be represented by the equation

$$M_s = \frac{M \cdot V_{dc\,mean}}{V_{dc\,real}}$$

…………………..(10)

where is the average value of the dc-link voltage and is the online dc-link voltage with 2nd harmonic ripple voltage on the dc bus, both per unit.

B. PERCENTAGE:

The percentage is a constant which is added to (10) to show the trace of the harmonics while the percentage of ripple in varies (i.e., when the method is not used / 0%) as in Fig. 6, or it is used as in Fig. 7 0%)

$$M_s = \frac{M \cdot V_{dc\,mean}}{V_{dc\,real} \cdot \frac{\Xi}{100}} \cdot$$

………………..(11)

Fig. 8 shows the curves of the most significant harmonics when the dc-link voltage has a ripple of 10% 2nd harmonic at 0.75, while varies from zero to 125% (i.e., when the dc-link ripple-voltage is 10% of the average dc-bus voltage and 100%), the ripple of the modulating signal with respect to the modulation index is 10%. The -axis represents the per-unit values of each harmonic over the fundamental component. It is observed that the third harmonic is rejected when is between 90 to 105% ripple on the modulating signal. Fig. 8 shows that the 3rd harmonic reduces as the ripple increases from zero to 95% and then increases again. The increase of the modulating signal's percentage increases the 15th, the 17th, and 19th harmonics.

C.EFFECT OF THE METHOD:

The immunity from the dc to ac side for extreme cases is investigated by using the repositioning technique. The case of the dc bus with 10% of the 2nd harmonic ripple voltage, shown in Fig. 9, is the first case. The individual voltage distortion limit for bus-voltage harmonics in power systems is 3% according to the industry standards [27]. Hence, 10% of 2nd harmonic ripple voltage is an extreme case, but is used as a way to illustrate the performance of the technique under this scenario.

The case of a dc bus with 10% of 4th harmonic ripple voltage is studied in [28]. However, it is beyond the scope of this paper to study the 4th harmonic content in the dc-link voltage. The 6th harmonic on the dc bus can be caused by three-phase rectification or even by the flow of non characteristic 5th and 7th harmonic current on the ac side. The typical value of the 6th harmonic is not higher than 3% of the dc-link voltage [27].
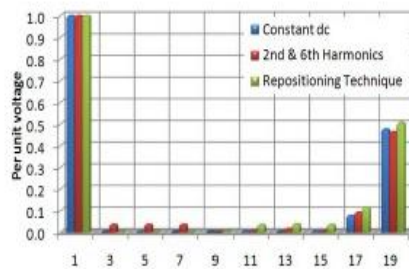

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Fig. 11. Per-unit values of the low-order harmonics up to the 19th for a dc bus with a ripple of 7.5% 2nd and 7.5% 6th harmonics
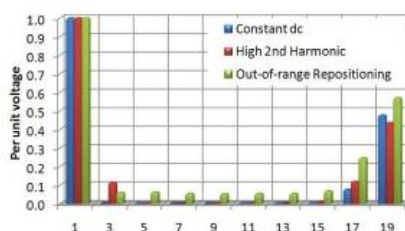

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Fig. 12. Per-unit values of the low-order harmonics up to the 19th for a dc bus with a ripple of 25% 2nd harmonic.

The extreme case of a dc bus with 10% 6th harmonic is examined in this section. A significant amount of 5th and 7th harmonics is produced at the ac network (Fig. 10). The repositioning technique eliminates the 5th and 7th harmonics but it produces 11th and 13th harmonics instead. The 11th harmonic is the reflection of the 7th one by applying the repositioning technique. That reflection is expected to be the midpoint between the fundamental component and the first significant harmonic since the technique is based on amplitude modulation. By applying the repositioning technique to an equivalent circuit with dc-bus ripple voltage above the midpoint, the technique is not beneficial. Hence, the frequencies which are closest to the first significant harmonic (i.e., 10th harmonic and above for the examples in this paper) need to be filtered out by using other methods. Fig. 11 shows the simulation results when the repositioning technique is applied to an equivalent circuit of dc-bus ripple voltage with the

combination of two harmonics. The most regular harmonics that are expected to fluctuate the dc bus are the 2nd and 6th. Hence, 7.5% of the 2nd and 7.5% of 6th harmonics are added to the dc bus. It is observed that the technique repositions the low-order harmonics even when the dc link fluctuates with a combination of harmonics.

The repositioning technique is also applied for a very high dc-bus ripple voltage, 25% of the 2nd harmonic. For the conventional SHE-PWM, a high value of the 3rd harmonic on the ac side is expected. Fig. 12 shows that when the repositioning technique is used above the range, a magnitude of every odd harmonic appears on the ac side. The constraint of the technique is to keep the modulating signal below the maximum modulation index.
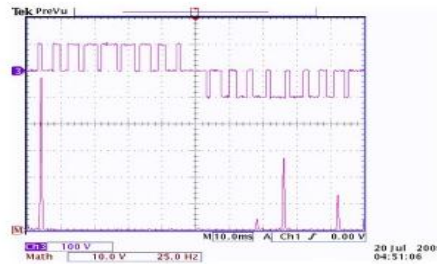

Fig. 13. Line-to-line voltage spectrum up to the 25th harmonic for a constant dc bus.

IV. Experimental Results:

The repositioning technique is verified by experimental results which are taken with a two-level three-phase VSC prototype, controlled by the ds1104 R&D Controller Board and with a 100-V dc-bus voltage. The dc–ac inverter operates at 10-Hz frequency using SHE-PWM [Fig. 3(d)]. The time-step of the real-time program is 50 s. The operating frequency of 10 Hz is selected to avoid additional harmonics being introduced in the signals due to the large time-step resolution of the real-time interface

The ac side is a star-connected load of 20 and 20 mH. Experimental results are shown in Figs. 13–17 proving the theory and the simulation results. Fig. 13 shows the line-to-
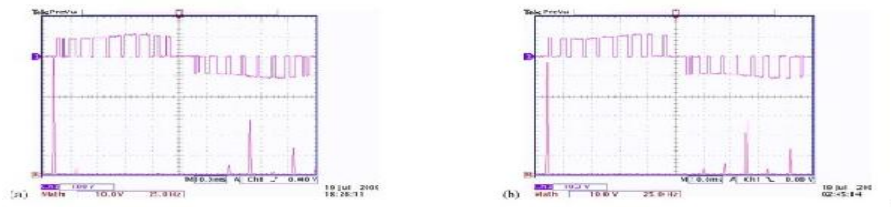

Fig. 14. Line-to-line voltage spectra for a dc bus with a ripple of (a) 10% 2nd harmonic without the repositioning technique and (b) when the technique is used.
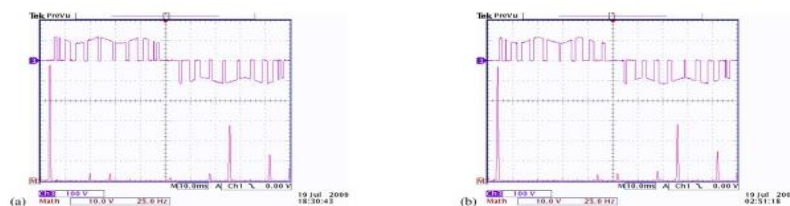

Fig. 15. Line-to-line voltage spectra for a dc bus with a ripple of (a) 10% 6th harmonic without the repositioning technique and (b) when the technique is used.
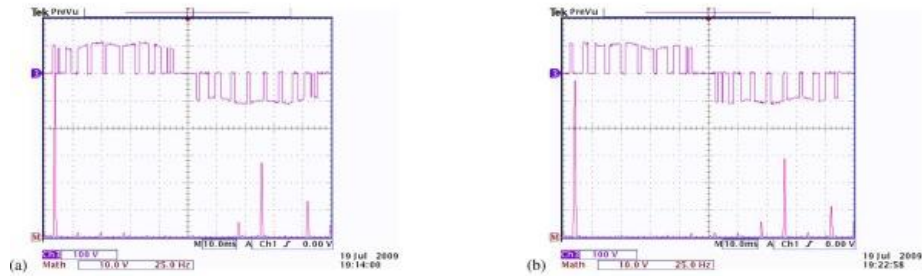
Fig. 16. Line-to-line voltage spectra for the dc bus with a ripple of 7.5% 2nd and 7.5% 6th harmonics without the repositioning technique and (b) when the technique is used.
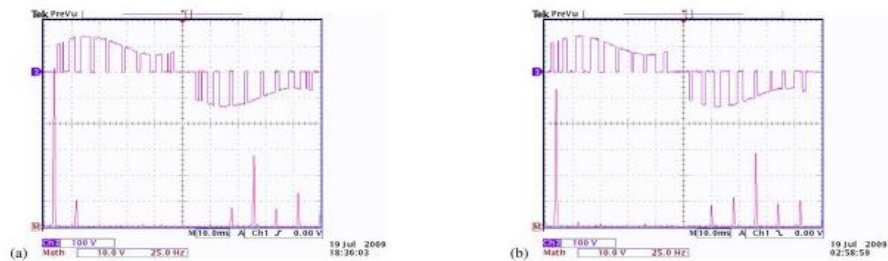

Fig. 17. Line-to-line voltage spectra for the dc bus with a ripple of 25% 2nd harmonic (a) without the repositioning technique and (b) when the technique is used.

Line voltage waveform and harmonic spectrum for SHE-PWM by using the repositioning technique for a constant dc bus. The voltage waveform and spectrum of Fig. 13 are identical to the results taken by the conventional SHE-PWM. Fig. 14(a) proves that the dc-link ripple voltage of the 2nd harmonic increases the fundamental and creates a 3rd harmonic to the line-to-line voltage. The repositioning technique regulates the fundamental component and eliminates the 3rd harmonic but increases the switching frequency and its sidebands, as observed by Fig. 14(b). As shown in Figs. 15 and 16, the technique also removes the 5th and 7th harmonics from the line-to-line voltage created by the 6th harmonic ripple voltage of the dc bus. Those ac-side harmonics are moved to the 11th and 13th harmonics.

The magnitude of the 5th and 7th harmonics is 5% of the fundamental and the magnitude of the reflected ones, 11th and 13th, are 5% of the switching frequency, which is much lower than the fundamental.

It is observed that the repositioning technique eliminates the low-order harmonics caused by the dc-bus ripple voltage when it satisfies the constraint . It is also observed that the fundamental component is increased when a second harmonic is added in phase for a conventional SHE-PWM. Using the repositioning technique, the magnitude of the fundamental is controlled. However, as shown in Fig. 17(b), when the technique is used out above the magnitude of the fundamental is lower than the required value but the harmonic spectrum is

V.   Conclusion:

An optimized SHE-PWM technique, which offers immunity between the ac and dc side in a two-level three-phase VSC, is discussed in this paper. The technique is highly significant in HVDCs due to the elimination of every low-order harmonic of the ac side produced by the dc-link ripple voltage. The dc-link ripple repositioning technique regulates the magnitude of the fundamental component and eliminates the low-order harmonics of the ac side even when the dc bus voltage fluctuates.

This is an online method which can be applied for eliminating any low-order harmonic frequency regardless of amplitude or phase shift of the ripple. There are some limitations related to the maximum modulation index available for SHE-PWM angles. The repositioning technique also causes a reflection with respect to the midpoint between the fundamental component and the first significant harmonic. There are cases where the technique is not beneficial. On the other hand, it eliminates all low-order ac-side harmonics for every dc-bus ripple voltage of frequency below the midpoint harmonic.

The future scope is it can extend into three phase three level VSC

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