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New Cascaded H-Bridge Multilevel Inverter Topology with Reduced Number of Switches and Sources

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Abstract : *In this paper mainly focused on the design and implementation of new topology in a single phase five level cascaded H-bridge multilevel inverter by using only a five switches and two DC power source. The main objective of this paper is to increase number of levels with a low number of switches and sources at the output without adding any complexity to the power circuit. The main merit of the new topology is to reduce the lower total harmonic distortion, lower electromagnetic interference generation and high output voltage. In this paper, various carrier pulse width modulation techniques are proposed, which can minimize the total harmonic distortion and enhances the output voltages from proposed work of five level inverter. The various switching topologies of single-phase five level cascaded H-bridge multilevel inverters have been analyzed in this paper. It is justified that the new topology can be recommended to single phase five level Cascaded H-bridge inverter for better performance in comparison with conventional method. The simulation is done by Mat Lab 8.0 version software.*

Index Terms*- cascaded H- bridge multilevel inverter, different phase pulse width modulation, low harmonics, MATLAB/Simulink software, reduced switches and sources.*

CHAPTER ORGANIZATION

I. INTRODUCTION

Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. The term Multilevel began with the three-level converter. The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975 [1]. In recent years multi level inverters are used high power and high voltage applications .Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multi level inverters are mainly classified as Diode clamped, Flying capacitor inverter and cascaded multi level inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor [2].There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another one is high switching frequency. For high switching frequency classified as space vector PWM, Selective Harmonics Elimination PWM and SPWM. Among these PWM methods SPWM is the most used for the multilevel inverter, because it has very simple and easy to implemented. In this paper present SPWM method with the different carrier based disposition PDPWM, PODPWM and APODPWM has been analyzed

[12] It is generally accepted that the PD strategy gives rise to the lowest harmonic distortion for the line-to-line voltage [13] [14].Any semiconductor switches have already been proposed.In this proposed concept uses the MOSFETs semiconductor switches. MOSFETs are preferred in: High frequency applications (1MHZ), Wide line or load variations, Long duty cycles, and Low-voltage applications (500V). Mainly selected the MOSFET switches are used because of its fast switching capability [15]

II. LITERATURE SURVEY

Based on the literature survey: we collect the many paper based on reduced the switches and sources in a single phase five level cascaded H-bridge multilevel

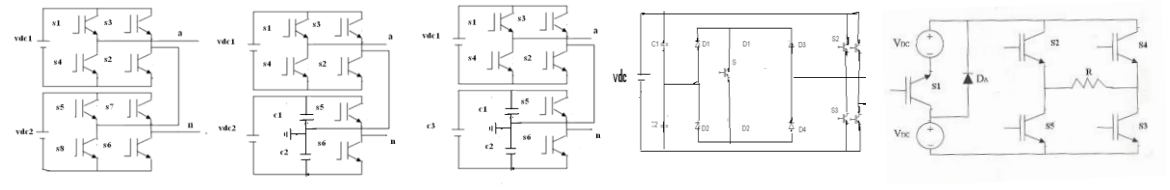
1. Cascaded H-bridge multilevel inverter using eight switches and two sources [3] [4]
2. Cascaded H-bridge multilevel inverter using eight switches and single source [5]
3. Cascaded H-bridge multilevel inverter using six switches and two sources [6] [7]
4. Cascaded H-bridge multilevel inverter using six switches and single source [8]
5. Cascaded H-bridge multilevel inverter using five switches and single source [9] [10]

In existing work, proposes the four level multilevel inverter by using six switches and two sources. Based on the existing work we are developed the new topology in a single phase five level cascaded H-bridge multilevel inverter by using a five switches and two sources [11]

III. CASCADED MULTILEVEL INVERTER TOPOLOGY

A cascaded multilevel inverter made up of from series connected single full bridge inverter,each with their own isolated dc bus.This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources,which may be obtained from solar cells, fuel cells,batteries,ultra capacitors, etc.This type of converter does not need any transformer or clamping diodes or flying capacitors [16].Each level can generate five different voltage outputs +2Vdc, +vdc, 0 ,–2Vdc and –vdc by connecting the dc sources to the ac output side by different combinations of the four switches.The output voltage of an M-level inverter is the sum of all the individual inverter outputs.Each of the H-Bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi- square waveform by phase-shifting its positive and negative phase legs switching timings.Further, each switching device always conducts for 180˚ (or half cycle)regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device [17].This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. A multilevel inverter has four main advantages over the conventional bipolar inverter.First,the voltage stress on each switch is decreased due to series connection of the switches.Therefore, the rated voltage and consequently the total power of the inverter could be safely increased.Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle.Third, harmonic distortion is reduced due to more output levels.Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained.[4].

IV. Various Switching Topologies Of Single Phase Five Level Cascaded H-Bridge Multilevel Inverter



(a) (b) (C) (d) (e)

Fig.1 single phase five level Multilevel cascade inverter using (a)eight switches and two sources (b) six Switches and two sources (c) six switches and single source (d) five switches and single source(e) Five switches and two source.

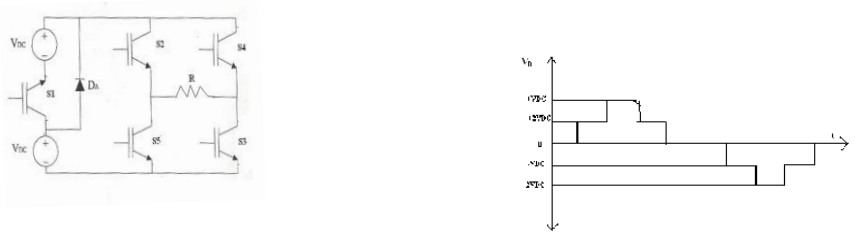
Table.1 comparison between different topologies with new proposed method of multilevel cascade inverter

TOPOLOGIES	SWITCHES	SOURCES	CAPACITORS	DIODES
FIRST TOPOLOGIES	8	2	-	-
SECOND TOPOLOGIES	6	2	2	-
THIRD TOPOLOGIES	6	1	3	-
FOUR TOPOLOGIES	5	1	2	4
NEW PROPOSED TOPOLOGIES	5	2	--	1

4.1 Principle of operation of Multilevel Cascade inverter

shows the circuit diagram of single phase five level cascaded H-bridge of various switching as shown in figure1 and they have the number of switches, diodes, and capacitors are comparison with proposed method of multilevel cascade inverter as shown in table1.especially shunt and series connected FACTS devices.The multilevel cascade inverter synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. A series of single-phase full bridges makes up a phase for the inverter. A single-phase multilevel cascade Inverter topology is essentially composed of single identical phase legs of the series-chain of H-bridge inverter, which can possibly generate different output voltage waveforms and offers the potential for ac system phase-balancing.This feature is impossible in other Voltage source control topologies utilizing a common dc link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge inverter is provided separately, and this is typically achieved using diode rectifiers without using the single-phase transformer.The converter topology is based on the series connection of single-phase inverters with separate dc sources the resulting phase voltage is synthesized by the addition of the voltages generated by the different cells.In a five level cascaded inverter each single-phase full-bridge inverter generates five voltages at the output:+Vdc, + 2vdc, 0,-Vdc and -2vdc.

V. Proposed Method Of Five Level Multilevel Cascaded H-Bridge Multilevel Inverter



(a) **(b)**

Fig. 2 proposed method of multilevel cascade inverter by using (a) five switches and two source (b) output waveform of five level multilevel inverter

5.1 PROPOSED METHOD OF STRUCTURES AND OPERATION

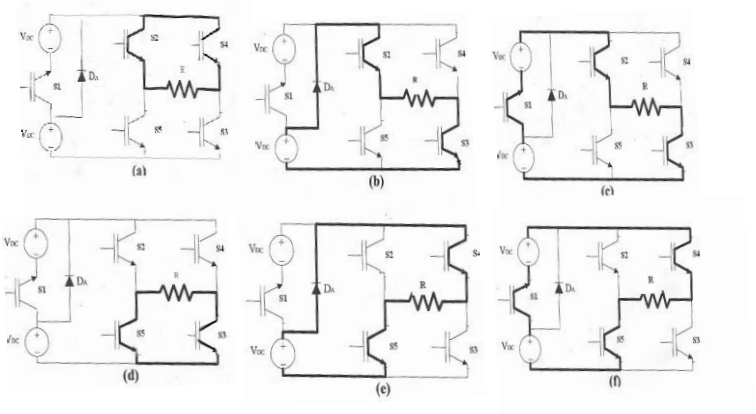


Fig.3 multilevel cascade inverter operation modes (a) 0 (b) vdc (c) -2vdc (d) 0 (e) –vdc (f) -2vdc
Table.2 showing the switching states of proposed method of five levels multilevel cascade inverter

OPERATION	DF	S1	S2	S3	S4	S5
0	OFF	OFF	ON	OFF	ON	OFF
VDC	ON	OFF	ON	ON	OFF	OFF
2VDC	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	ON	OFF	ON
-VDC	ON	OFF	OFF	OFF	ON	ON
-2VDC	OFF	ON	OFF	OFF	ON	ON

5.2 CONSTRUCTION AND OPERATION OF PROPOSED METHOD

The circuit diagram of proposed method of multilevel cascade inverter as shown in Figure 2.The circuit diagram of operation mode with proposed method of single phase five level cascaded H-Bridge multilevel inverter is shown in figure 3 and table 2.It consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four POWER MOSFET switches.The inverter produces output voltage in five levels: zero, Vdc, 2Vdc, 0,-Vdc and -2Vdc.The advantages of the inverter topology are: Improved output voltage quality,Smaller filter size,Lower Electromagnetic interferences,Lower total harmonics distortion compared with conventional five level pulse width modulation ,Reduced number of switches compared to the conventional 5-level inverter.The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform.Each H-bridge inverter is connected to its own dc source V_{dc}. By cascading the ac outputs of each H bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, each H-bridge inverter can produce five different voltages: When a switch S2 and S4 of one particular H-bridge inverter are closed, the output voltage is 0 .When a switch S2 and S5 are closed, the output voltage is $+V_{dc.}$ When a switch S1, S2 and S5 are closed, the output voltage is $+2V_{dc.}$. When a switch S3 and S5 are closed, the output voltage is 0 when a switch S4 and S5 of one particular H-bridge inverter are closed, the output voltage is $-V_{dc}$. When a switch S4 and S5 are closed, the output voltage is $+2V_{dc.}$ .Where the i stands for one particular H-bridge inverter.Therefore, to obtain the total ac voltage produced by the multilevel inverter, these five distinct ac voltages are added together.The one notices that five distinct dc sources can produce a maximum of 5 distinct levels in the output phase voltage of the multilevel inverter.More generally, a cascaded H-bridges multilevel inverter using separate dc sources can produce a maximum of S'= 4+(N-1) distinct levels in the output phase voltage

5.1 MULTILEVEL CASCADE INVERTER IS DISSCUSSED TO ELIMINATE

(1) Bulky transformers required by conventional multi pulse inverters,
(2) Clamping diodes required by multilevel diode-clamped inverters, and
(3) Flying capacitors required by multilevel flying-capacitor inverters.

5.2 FEATURES OF MULTILEVEL CASCADE INVERTER

(1) It is much more suitable to high-voltage, high-power applications than the conventional inverters.
(2). It switches each device only once per line cycle and generates a multistep staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels.
(3). since the inverter structure itself consists of a cascade connection of many single-phase, full-bridge Inverter units and each bridge is fed with a separate DC source, it does not require voltage balance circuits or voltage matching of the switching devices.

VI. Modelling Of Single Phase Five Level Cascaded H- Bridge Inverter

For each full bridge inverter the output voltage is given by

$$V0i = Vdc\,(S1i - S2i) \qquad (1)$$

And the input dc current is

$$Idci = Ia\,(S1i - S2i) \qquad (2)$$

Where,

(a) i =1…5 (number of full bridge inverters employed) for the 5 level type.
(b) I_{am} is the output current of the cascaded inverter.
(c) S_{1i} and S_{2i} is the upper switch of each full bridge inverter.

Now the output voltage of each phase of the multilevel cascaded inverter is given by:

$$V_{0n} = \sum V_{0i} \quad i = 1, 2....n \qquad (3)$$

In multilevel inverters, the amplitude modulation index (m_a) is the ratio of reference amplitude (a_M) to carrier amplitude (A_C).

$$m_a = A_m / (m-1) A_c \qquad (4)$$

The frequency ratio (m_f) is ratio of carrier frequency (f_C) to reference frequency (f_m).

$$m_f = f_c / f_m \qquad (5)$$

VII. Modulation Techniques For Multilevel Inverter

7.1 Definition of Modulation

Mainly the power electronic converters are operated in the "switched mode". This means the switches within the converter are always in either one of the two states - turned off or turned on. Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states.This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal.The switched component is attenuated and the desired dc or low frequency ac component is retained.This process is called Pulse Width Modulation, since the desired average value is controlled by modulating the width of the pulses.For maximum attenuation of the switching component, the switch frequency fc should be high- many times the frequency of the desired fundamental ac component f1 seen at the input or output terminals.In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses.For POWER MOSFET converters, the ratio of switch frequency to fundamental frequency fc/f1 may be as low as unity,which is known as square wave switching.Another application where the pulse number may be low is in converters which are better described as amplifiers ,whose upper output fundamental frequency may be relatively high.These high power switch-mode amplifiers find application in active power filtering, test signal generation, servo and audio amplifiers.These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible.The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible.In these circumstances, multi-level converters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall converter.

7.2 PULSE WIDTH MODULATION

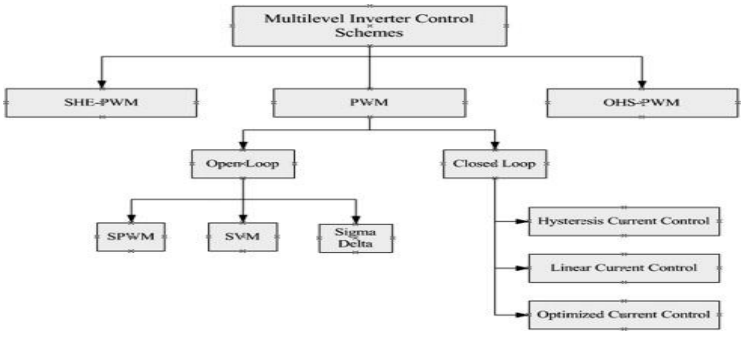


Fig. 4 classification of multilevel inverter control techniques

The fundamental methods of pulse-width modulation are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor or programmable logic device implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations.Both modulation schemes can be applied to the cascaded H-bridge

inverters.Total harmonics distortion of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation.An m-level multilevel inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers,all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous.There are three alternative Pulses with different phase relationships for the level-shifted multicarrier modulation three alternative carrier disposition Pulse width modulation strategies are commonly referenced, viz:

(i) Alternative phase opposition disposition, where each carrier is phase shifted by π from its adjacent Carrier [12].

(ii), Phase opposition disposition where the carriers above the sinusoidal reference zero point are π Out of phase with those below the zero point [12]

(iii) Phase disposition, where all carriers are in phase [12].

7.3 Alternate Phase Opposition Disposition (APOD)

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 1800. Since APOD and POD schemes in case of five-level inverter are the same, a five level inverter is considered to discuss about the APOD scheme.The rules for APOD method, when the number of level N = 5, are

1. The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its carrier by 180. The converter switches to +I vdc when the reference is greater than all the carrier waveforms.
2. The converter switches to 2 vdc when the reference is less than the uppermost carrier waveform and greater than all other carriers
3. The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greatest than lowermost carrier.
4. The converter switches to – 1 vdc when the reference is greater than the lowermost carrier waveform and lesser than all other carriers
5. The converter switches to -2 vdc when the reference is lesser than all the carrier waveforms : Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter: Four triangles and the modulation signal

7.4 PHASE OPPOSITION DISPOSITION

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180° out of phase with those below zero. The rules for the phase opposition disposition method, when the number of level N = 5

1. The N –1 = 4 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180 out of phase with those below zero
2. The converter is switched to + Vdc when the reference is greater than both carrier waveforms.
3. The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
4. The converter is switched to +2Vdc when the reference is less than both carrier waveforms.
5. When the modulation signal is greater than both the carrier waveforms, S1 and S2 are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S2and S1 are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S1an and S2an are turned on and the converter switches to negative node voltage.

7.5. IN Phase Disposition

There in, the a-phase modulation signal is compared with two triangle waveforms. The rules for the in phase disposition method, when the number of level N = 5, are

1. The N –1 = 5-1= 4 carrier waveforms are arranged so that every carrier is in phase.
2. The converter is switched to +Vdc when the reference is greater than both carrier waveforms.
3. The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
4. The converter is switched to 2Vdc when the reference is less than both carrier waveforms

VIII. Simulation Of The Various Switiching Topologies In A Single Phase Five Level Multilevel Cascade Inveter

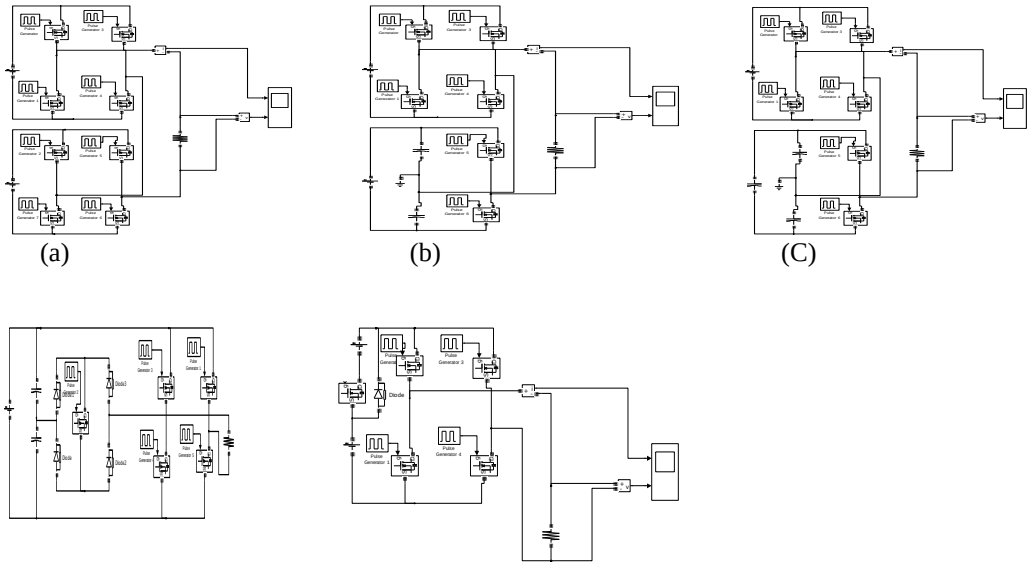


Fig 5 showing simulation results of single phase five level Multilevel cascade inverter using(a)eight switches and two sources (b) six Switches and two sources (c) six switches and single source (d) five switches and single source (e) five switches and two sources .

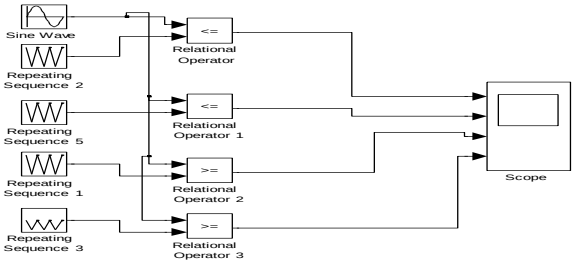
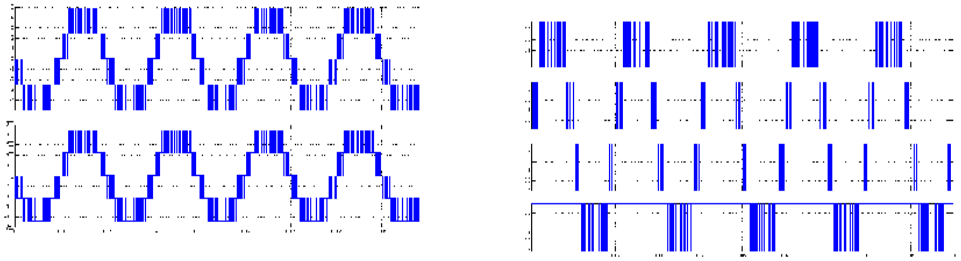
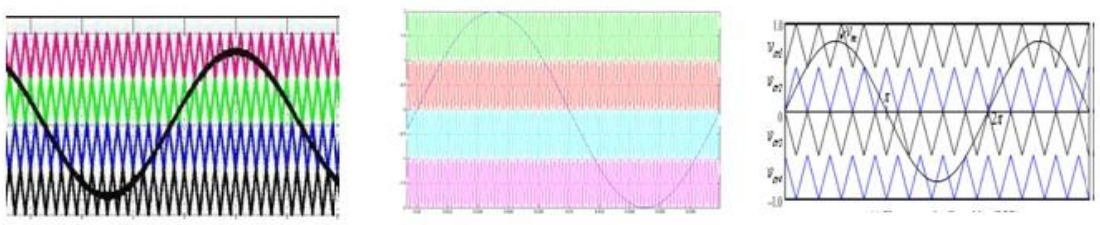


Fig 6 showing the circuit diagram of pulse width modulation of single phase five level multilevel cascade inverter



(a) **(b)**

Fig 7 showing the simulation results of five level multilevel cascade inverter (a) output waveform of all Five level inverter (b) pulse generated pwm



(a) (b) (C)

Fig 8 showing the simulation results of five levels MCI (a) APODPWM (b) PDPWM (c) PODPWM

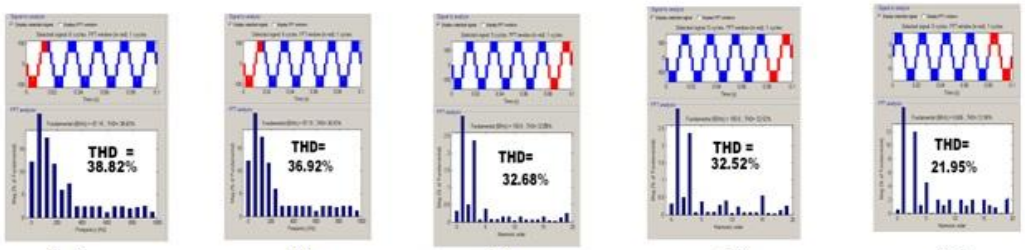


FIG 9 SHOWING THE SIMULATION RESULTS OF MULTILEVEL CASCADE INVERTER (a) using 8 switches and 2 sources THD is 38.82% (b) using 6 switches and 2 sources THD is 36.92%(c) using 6 switches and 1 sources THD is 32.68% (d) using 5 switches and 1 sources THD is 32.52%(e) using 5 switches and 2 sources THD is 21.95%

IX. Simulation Results Comparison

In this section the different topologies single phase five level multilevel cascade inverter simulation results can be shown with R-load by using the phase disposition pulse width modulation techniques.

The comparison of simulation results are shown in Table 3

MULTILEVEL CASCADE INVERTER USING 8 SWITCHES	MULTILEVEL CASCADE INVERTER USING 6 SWITCHES	MULTILEVEL CASCADE INVERTER USING 6 SWITCHES AND 1 SOURCES	MULTILEVEL CASCADE INVERTER USING 5 SWITCHES AND 1 SOURCES	MULTILEVEL CASCADE INVERTER USING 5 SWITCHES AND 2 SOURCES
38.82%	36.92%	32.68%	32.52%	21.95%

The various Carrier-Based techniques such as PD, POD, and APOD are analyzed and the simulation results of different method of multilevel cascade inverter are tabulated.In this chapter the different Carrier based techniques implemented with different topologies.The results of multilevel cascade inverter with R-load by using different topologies of multilevel cascade inverter are obtained. The conclusion from this table is from all the above techniques the Phase Disposition (PD) have the low harmonic distortion. So the proposed method of multilevel cascade inverter we uses the Phase Disposition pulse width modulation. A summary of THD for Cascaded multilevel inverter by using different modulation techniques is presented. Cascaded five-level inverter is simulated for modified reference with triangular carriers and modified reference with modified carrier.The simulation results for output voltage with harmonic spectrum are presented, it is concluded that Cascaded five-level inverter of proposed work with different modulation technique has good harmonic spectrum with THD (21.95 %) for the switching frequency of 1 KHz .

The comparison of phase disposition pulse width modulation techniques of different method in MCI are shown in Table 4

MCI BY USING	PDPWM	PODPWM	APODPWM
8 SWITCHES AND 2 SOURCES	38.82	39.45	39 .97
6 SWITCHES AND 2 SOURCES	36.92	37.34	37.56
6 SWITCHES AND 1 SOURCES	32.68	33.16	34.23
5 SWITCHES AND 1 SOURCES	32.52	33.07	34.16
5 SWITCHES AND 2 SOURCES	21.95	22.13	24.85

In this section the proposed method of single phase five level multilevel cascade inverter simulation results can be shown with R-load by using the different phase disposition pulse width modulation techniques

The comparison of simulation results are shown in Table 5

MI	PDPWM	PODPWM	APODPWM
0.4	21.95	22.13	24.85
0.6	18.54	21.45	23.65
0.8	17.12	20.78	22.43
1.0	15.89	19.67	21.21
1.2	14.08	18.56	20.57

X. Experimental Results

experimentally validate the multilevel cascde inverter using the four switches and single sources with phase disposition pulse width modulation, a prototype five level multilevel cascade inverter has been built using POWER MOSFET for the full bridge inverter as shown in below .The gating signals are generated using phase Disposition pulse modulation the hardware implementation of proposed method of multilevel cascade inverter is shown in Fig.10

FIGURE 10 SHOWING THE HARDWARE MODEL OF PROPOSED METHOD

10.1 HARDWARE DESCRIPITION

1. AC SOURCES one Transformers of 230V for individual sources of single H-bridges
2. Transformers for one H-bridges, to supply VCC for various ICs used as optocouplers and comparators Voltage rating - 500V -Current rating – 40A
3. Four POWER MOSFET SWITCHES IS USED
4. To generate the firing pulses of proposed method phase disposition pulse width modulation technique OPTOCOUPLERS (4506) - COMPARATORS (IC 4081)
5. LOAD - Single Phase
6. R load = 30 ohms

10.2 Hardware Results

1. Proposed Topology: Single phase Cascaded 5-level H-bridge Inverter using 4 switiches and 1 sources
2. Input Voltage: 230V
3. Switching Frequency: 1 KHz

4. Nature of output: 5-levels

In this section the proposed method of single phase five level multilevel cascade inverter hardware results can be shown with R-load by using the different phase disposition pulse width modulation techniques.

The comparison of hardware results are shown in Table 6

MI	PDPWM	PODPWM	APODPWM
0.4	21.20	21.23	24.05
0.6	17.54	21.02	23.15
0.8	16.32	20.16	22.53
1.0	15.12	19.18	21.01
1.2	14.04	18.16	20.17

XI. Conculsion

Prototype of the 5-level single-phase multilevel cascaded inverter consists of a single-phase inverter and single H-bridge inverters that it uses separate dc power sources. The control signals for power electronic switches are by using different pulse width modulation modulated technique. In this paper both simulation results and hardware prototype model results are correlated. Harmonic analysis carried out using Mat Lab 8.0 version software .It is proved that proposed work of Single phase five level multilevel cascade inverter output voltage total harmonics distortion is reduced and improve the efffienicy of system compare with different topologies of single phase five level multilevel cascade inverter . It is also proved that low total harmonics distortion in phase disposition pulse modulation compared to Phase opposition disposition pulse width modulation and Alternate phase opposition disposition pulse width modulation of multilevel cascade inverter. Future plan is to implementated both simulation and hardware prototype model of the closed loop of single phase five level multilevel cascade Inverter.

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