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Three Phase Digitally Controlled Power Factor Improvement System

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Abstract: *This paper presents a simple design of digital control circuit for three phase power factor improvement system. The approach is based on the determination of a count representing a number of pulses which is proportional to both the phase shift between the line voltage and the line current, and the load current. This count addresses a ROM which is programmed with pre – calculated switching combinations of "0_S and 1_S" switch the required capacitors or any other combinations network to the system to improve the power factor. A time sharing switching circuit is designed so as to scan the three phases sequentially to determine power factor for each phase using the same control circuit. Power factor improvements up to 0.95 have been obtained for maximum load of 20A.*

The same control circuit can be implemented for higher loads with very minor alterations, i.e. altering the switching combinations stored in the ROM and changing the current rating of the Triacs.

Keywords: *Power Factor improvement, Triac Switching Digital Control, Instrumentation.*

I. Introduction

The high cost of energy generation, transmission and distribution and their difficulties in my country Iraq has necessitated the search for means to achieve better efficiency of utilization of power systems. Power factor improvement is a very good way to increase the usage of existing power to full use. Many researchers [1-10] have carried out work in this field producing different types of designs. There are different methods of power factor correction implemented with large lagging or leading non linear loads [1]. Many researchers use a variable inductor in parallel with a fixed capacitor as reactive power compensating circuit [2-3]. The inductor current is controlled by adjusting the firing angle of two anti – parallel connected thyristors or using TRIAC [4]. One of the new approaches [5] is to use a single large capacitor to improve the power factor. The voltage across this capacitor is controlled by a bidirectional switch, which is continuously on\off by a pulse width modulated (PWM) signal of moderately high frequency.

The proposed system is more reliable because it involves the counts of the lagging current in the power factor with a very accurate and precise setting, in terms of calculating the phase angle in the power system, so that the power factor of the load will always be maintained around a certain predetermined value. The interval between each two switching operations can be set anywhere in the range between 20ms and few minutes using a binary ripple counter. This will minimize the effect of switching transients on the network under control.

II. Theoretical Background of the proposed Scheme

The control circuit of the system is designed to count a number of pulses proportional to both power factor and load current. This number is used to define the capacitance required to improve the load power factor to a pre – selected value. A voltage to frequency converter (VFC) is used to generate clock pulses with frequency F_C α I, where I is the load current, hence $F_C = K_1 \times I$. Where K_1 is a constant determined by the transformation ratio of the current transformer, gain of the precision rectifier and conversion constant of the VFC. The number of clock pulses generated in the period of phase differences is counted as

$$N = N_P \frac{\phi}{2\pi}$$

where $N_P = \frac{F_C}{F_m}$ Where F_m is the frequency of the main supply and ø is the phase angle.

$$N = \frac{\phi}{2\pi}\frac{F_c}{F_m}$$

$$= \frac{K_1}{2\pi F_m} I\phi$$

where $F_c = K_1 I$

$$\mathrm{N} = \mathrm{KI}\phi \qquad (1)$$

where $K = \frac{K_1}{2\pi F_m}$

Hence the number of clock pulses (N) generated in the period of the phase difference is proportional to the product of (I×ø).
Using eqn (1)

$I_X = I\sin\phi = \frac{N}{K}\frac{\sin\phi}{\phi}$ Where I_x = reactive current of the load

Since N is a function of both ø and I, then for each value of N there is a range of values of the reactive current *I sinø*, this range is a function of

$\frac{\sin\phi}{\phi}$

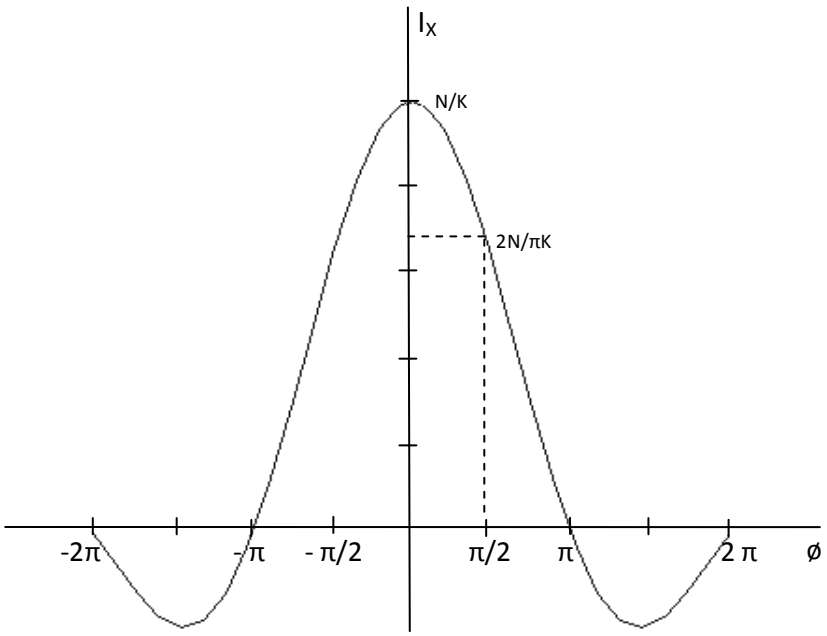

Fig (1) Variation of I_X with ø

Since the power factor of any actual load may vary from 0 to 90 degrees, then the values of *I sinø* at these limits are given as

$$\lim_{\phi\to 0} I\sin\phi = \lim_{\phi\to 0}\frac{N}{K}\frac{\sin\phi}{\phi}$$

$$= \frac{N}{K} \qquad (2)$$

$$\text{also } \lim_{\phi\to\frac{\pi}{2}} I\sin\phi = \lim_{\phi\to\frac{\pi}{2}}\frac{N}{K}\frac{\sin\phi}{\phi}$$

$$= \frac{N}{K}\frac{2}{\pi}$$

$$= 0.637\frac{N}{K} \qquad (3)$$

This range varies between a maximum value (N/K) when ø = 0 degree, and a minimum value (0.637 N/K) when ø = 90 degree.

Therefore, at each value of N a suitable combination of capacitors can be used for the correction such that capacitive current is around the minimum value given in equation (3), thus the possibility of over – compensation is eliminated. The above theory was used to calculate the capacitance required and the switching combinations to be stored in the ROM (see table 1).

Table 1. Switching combinations stored in ROM

Address	**Information Stored in ROM (HEX)**															
0000	FF	FF	FF	FF	FE	FE	FE	FE	FD	FD	FD	FB	FB	FB	FB	FB
0010	FC	FC	FC	FC	FA	FA	FA	FA	F9	F9	F9	F9	F5	F5	F5	F5
0020	F8	F8	F8	F8	F4	F4	F4	F4	F3	F3	F3	F3	F2	F2	F2	F2
0030	F2	F2	F2	F2	F0	F0	F0	F0	F0	F0	F0	F0	F0	EF	EF	EF
0040	EF	EE	EE	EE	EE	ED	ED	ED	ED	EB	EB	EB	EB	EC	EC	EC
0050	EC	EA	EA	EA	EA	E9	E9	E9	E9	E5	E5	E5	E5	E8	E8	E8
0060	E8	E4	E4	E4	E4	E2	E2	E2	E2	E1	E1	E1	E1	FF	FF	FF
0070	The Rest of the ROM is Empty															

III. System Hardware

3.1- Controller Circuit

As mentioned in section 2 the system correction is based on the determination of a binary count representing a number of pulses which is proportional to the magnitude of the current and the phase shift between the line voltage and line current.

The required hardware consists of squaring amplifier, EXCLUSIVE – OR, AND gates, voltage to frequency converter (VFC), counters and ROM.

Squaring amplifiers are used to make the line voltage and line current signals compatible with TTL logic circuits. These two signals are EXCLUSIVE – ORed to produce pulses of duration equal to the phase difference. VFC is used to provide a signal of frequency proportional to the magnitude of the load current. The output from the EXCLUSIVE – OR and VFC stages are ANDed together, producing a train of pulses similar to that of the EXCLUSIVE – OR gate stage with clock pulses imbedded in it.

The number of clock pulses imbedded in the interval of the phase differences will thus represents both the phase angle and the current magnitude, i.e. I&ø.

The switching combinations have been pre – calculated in accordance with the frequency range and transformation constant of the VFC, and the phase angle range between the line voltage and current of the load under control. The above description is best illustrated with reference to the block diagram of the controller circuit Fig. (2) and the timing diagram Fig. (3).

The case of over compensation (which might occur) has been taken into consideration, thus the system is equipped with a Lead/Lag detector, which will disable compensation at any "Lead" instant. The Lead /Lag detector is built around a "D" type flip flop as shown in Fig. (6).

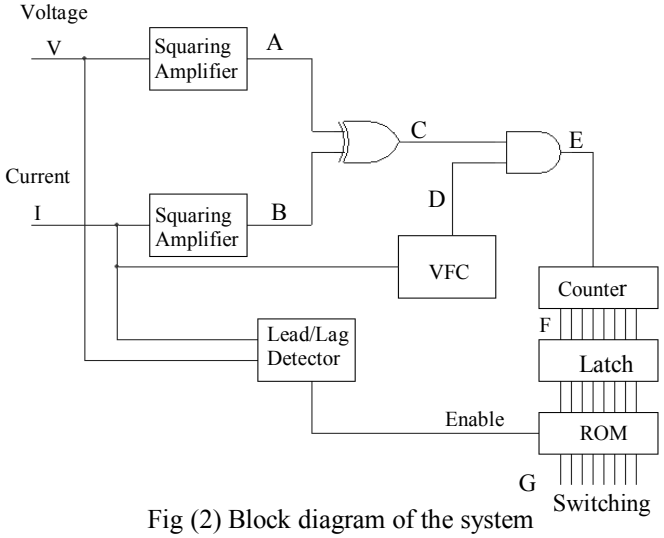

Fig (2) Block diagram of the system

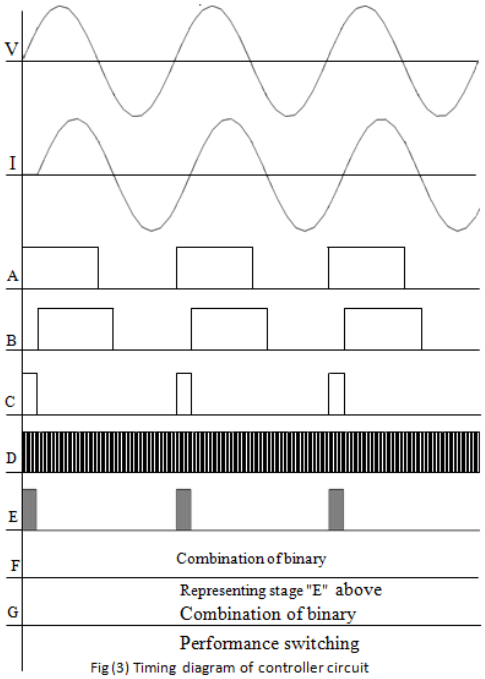

Fig (3) Timing diagram of controller circuit

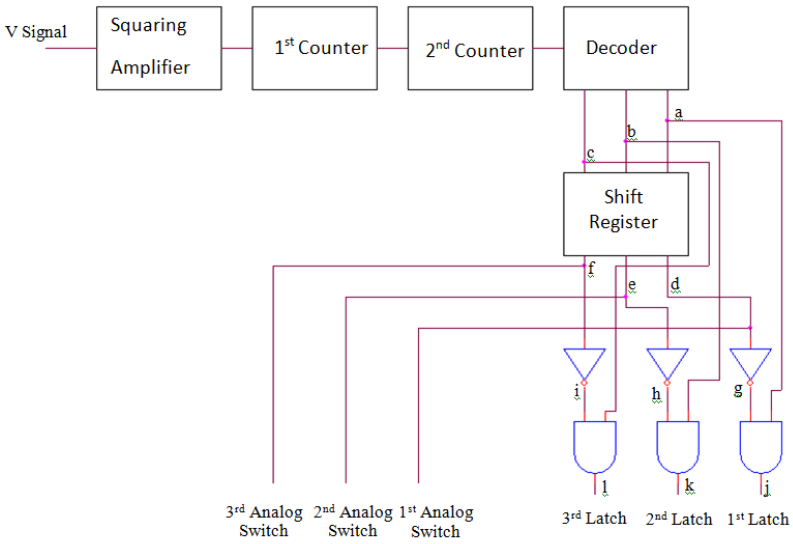

Fig (4) Time sharing circuit

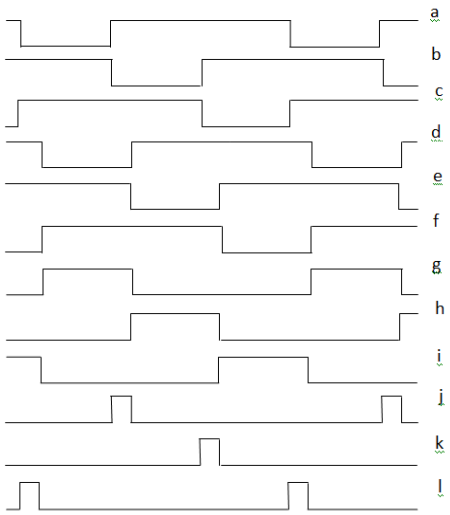

Fig (5) Timing diagram of time sharing circuit

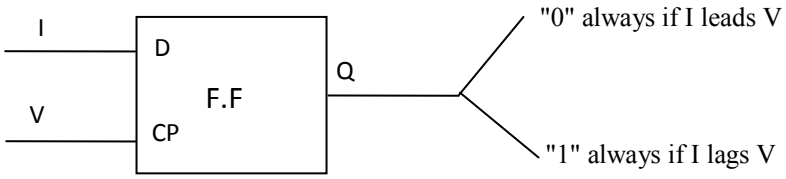

Fig (6) Lead/Lag detector

3.2 Time Sharing Circuit

Three phase power factor correction is achieved by using the time sharing circuit designed so as to scan the three phases sequentially by using the same control circuit.

The circuit consists of squaring amplifier, counters, decoder, shift registers, inverters, and AND gates (see fig. 4). Clock pulses compatible with T.T.L logic circuit are obtained by using squaring amplifier to shape line voltage signal and limit its level to that of T.T.L logic circuits. These pulses are fed to the first counter to define the scanning period. One of the output bits of the first counter is used as the clock to the second counter, which is connected in such away with a decoder to obtain three stable states only. Thus the individual period is decided by the first counter depending on the bit used.

To obtain three states suitable for latching the output of the control circuit (fig. 4, a, b, c) these states are shifted, inverted and ANDed with itself. The current and voltage of each phases is fed through analog switch controlled by the first output of the shift register.

IV. Conclusion

The prototype of the system was subjected to various types of load, within the rated current of the design, i.e. 20A. Good resolution and accuracy were obtained, when the power factor improvement up to 0.95 have been achieved at different load currents. Five capacitors of the following values were used; 5µF, 10µF, 20µF, 40µF, 80µF with 300V. This combination can give a total capacitance between 5µF and 155µF in steps of 5µF, which is thought to be more advantageous and flexible than using capacitors of the same rating. The maximum designed line current have been taken to be 20A, 50Hz, but this does not limit the use of the new design because it is only required to replace the switching triacs with others of higher current rating, and also changing the switching combinations stored in the ROM accordingly.

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